RELIABILITY REPORT

FOR

MAX9867ETJ+T / MAX9867EWV+T

PLASTIC ENCAPSULATED DEVICES

November 26, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Manager, Reliability Operations

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Conclusion

The MAX9867ETJ+T / MAX9867EWV+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9867 is an ultra-low power stereo audio codec designed for portable consumer devices such as mobile phones and portable gaming consoles. The device features stereo differential microphone inputs that can be connected to either analog or digital microphones. The single-ended line inputs, with configurable preamplifier, can be sent to the ADC for record or routed directly to the headphone amplifier for playback. An auxiliary ADC path can be used to track any DC voltage. The stereo headphone amplifiers support differential, single-ended, and capacitorless output configurations. Using the capacitorless output configuration, the device can output 10mW into 32 headphones. Comprehensive click-and-pop circuitry suppresses audible clicks and pops during volume changes and startup or shutdown. Utilizing Maxim's proprietary digital circuitry, the device can accept any available 10MHz to 60MHz system clock. This architecture eliminates the need for an external PLL and multiple crystal oscillators. The stereo ADC and DAC paths provide user-configurable voiceband or audioband digital filters. Voiceband filters provide extra attenuation at the GSM packet frequency and greater than 70dB stopband attenuation at fS/2. The MAX9867 operates from a single 1.8V supply, and supports a 1.65V to 3.6V logic level. An I²C 2-wire serial interface provides control for volume levels, signal mixing, and general operating modes. The MAX9867 is available in a tiny 2.2mm x 2.7mm, 0.4mm-ball-pitch, WLP package. A 32-pin 5mm x 5mm TQFN package is also available.

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II. Manufacturing Information

A. Description/Function:	Low-Power, Stereo Audio Codec	
B. Process:	CMOS	
C. Number of Device Transistors:	410720	
D. Fabrication Location:	Taiwan	
E. Assembly Location:	China and Thailand	Japan
F. Date of Initial Production:	April 25, 2009	

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5	30-bump WLP 5X6
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	N/A
D. Die Attach:	Conductive	None
E. Bondwire:	Au (1 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	None
G. Assembly Diagram:	#05-9000-3197	#05-9000-3539
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	47°C/W	N/A°C/W
K. Single Layer Theta Jc:	1.7°C/W	N/A°C/W
L. Multi Layer Theta Ja:	29°C/W	49 °C/W
M. Multi Layer Theta Jc:	1.7°C/W	N/A°C/W

IV. Die Information

A. Dimensions:	89.37 X 107.09 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Operations) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QNIZDA004B, D/C 0909)

The AU97 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 1500V per JEDEC JESD22-A114
ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1

Reliability Evaluation Test Results

MAX9867ETJ+T / MAX9867EWV+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	QNIZDA004B, D/C 0909

Note 1: Life Test Data may represent plastic DIP qualification lots.

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