

RELIABILITY REPORT  
FOR  
MAX98400BETG+  
PLASTIC ENCAPSULATED DEVICES

October 2, 2012

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

<b>Approved by</b>
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Quality Assurance
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## Conclusion

The MAX98400BETG+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX98400A/MAX98400B Class D amplifiers provide high-performance, thermally efficient amplifier solutions. The MAX98400A delivers 2x20W into 8 loads or 1x40W into a 4 load. The MAX98400B delivers 2x12W into 8 loads. An integrated limiting circuit prevents output clipping distortion, protects small speakers from transient voltages, and reduces power dissipation. A thermal-foldback feature can be enabled to automatically reduce the output power at above a junction temperature of +120°C. Traditional thermal protection is also available in addition to robust overcurrent protection. The ICs operate from a single 8V to 28V supply and provide a high 67dB PSRR, eliminating the need for a regulated power supply. They offer up to 90% efficiency from a 12V supply. Filterless modulation allows the ICs to pass EN55022B EMI limits with 1m cables using only a low-cost ferrite bead and small-value capacitor on each output. Both devices feature eight-digitally-controlled gain settings. Comprehensive click-and-pop reduction circuitry minimizes noise coming into and out of shutdown. The MAX98400A/MAX98400B are available in 36-pin and 24-pin TQFN packages, respectively, and are specified over the -40°C to +85°C temperature range.

**II. Manufacturing Information**

A. Description/Function:	Stereo, High-Power, Class D Amplifier
B. Process:	S18
C. Number of Device Transistors:	3390
D. Fabrication Location:	Texas, California, Japan
E. Assembly Location:	Taiwan, Thailand
F. Date of Initial Production:	June 25, 2010

**III. Packaging Information**

A. Package Type:	24L TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3977 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	3°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	3°C/W

**IV. Die Information**

A. Dimensions:	100 X 95.28 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18μm
F. Minimum Metal Spacing:	0.18μm
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
 Don Lipps (Manager, Reliability Engineering)  
 Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 4340 \times 190 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 1.1 \times 10^{-9}$$

$$\lambda = 1.1 \text{ F.I.T. (60\% confidence level @ } 25^{\circ}\text{C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (Latch-Up lot SD7ZDA006A, D/C 1108)

The AX18 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2000V per JEDEC JESD22-A114	Lot ED7ZEQ001A, D/C 1125
ESD-CDM:	+/- 750V per JEDEC JESD22-C101	Lot SD7ZDA006A, D/C 1108

Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX98400BETG+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C	DC Parameters	72	0	TD7ZFZ014B, D/C 1214
	Biased	& functionality	70	0	TD7ZFZ008B, D/C 1201
	Time = 1000 hrs.		48	0	SD7ZC3001B, D/C 1214

Note 1: Life Test Data may represent plastic DIP qualification lots.