RELIABILITY REPORT FOR

MAX98358ETE+T / MAX98358EWL+T

PLASTIC ENCAPSULATED DEVICES

November 5, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX98358ETE+T / MAX98358EWL+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX98358 is a digital pulse-density modulated (PDM) input Class D power amplifier that provides Class AB audio performance with Class D efficiency. This IC offers five selectable gain settings (3dB, 6dB, 9dB, 12dB, and 15dB) set by a single gain-select input (GAIN). The IC can be configured to produce a left channel, right channel, or (left/2 + right/2) output from the stereo input data. The MAX98358 takes a stereo pulse density modulated (SPDM) input signal directly into the DAC. Data on the rising edge of PDM_CLK is considered left-channel data while data on the falling PDM_CLK edge is right channel. A mono sum feature is also implemented with SPDM data input by summing the data from both rising and falling clock edges. Active emissions-limiting, edge-rate limiting, and overshoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices and reduces the component count of the solution. The IC is available in 9-pin WLP (1.345mm x 1.435mm x 0.64mm) and 16-pin TQFN (3mm x 3mm x 0.75mm) packages and is specified over the -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	PDM Input Class D Audio Power Amplifier	
B. Process:	S18	
C. Number of Device Transistors:	159812	
D. Fabrication Location:	USA	
E. Assembly Location:	Taiwan, China, Thailand	USA
F. Date of Initial Production:	September 27, 2013	September 27, 2013

III. Packaging Information

A. Package Type:	16-pin TQFN 3x3	91-bump WLP
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	N/A
D. Die Attach:	Conductive	None
E. Bondwire:	Au (1.3 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	None
G. Assembly Diagram:	#05-9000-5403	#05-9000-5402
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	64°C/W	N/A°C/W
K. Single Layer Theta Jc:	6.9°C/W	N/A°C/W
L. Multi Layer Theta Ja:	48°C/W	73°C/W
M. Multi Layer Theta Jc:	6.9°C/W	N/A°C/W

IV. Die Information

A. Dimensions:	57.874 X 54.3307 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EANZ7Q002, D/C 1335)

The AX76-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114
ESD-CDM: +/- 500V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX98358ETE+T / MAX98358EWL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	EANZ7Q002F, D/C 1335

Note 1: Life Test Data may represent plastic DIP qualification lots.

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