RELIABILITY REPORT

FOR

MAX98356EWL+T

WAFER LEVEL PRODUCTS

February 14, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX98356EWL+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX98356 is a digital pulse-density modulated (PDM) input Class D power amplifier that provides Class AB audio performance with Class D efficiency. This IC offers five selectable gain settings (3dB, 6dB, 9dB, 12dB, and 15dB) set by a single gain-select input (GAIN). The MAX98356 takes a stereo pulse density modulated (SPDM) input signal directly into the DAC. Data on the rising edge of PDM_CLK is considered left-channel data while data on the falling PDM_CLK edge is right channel. The IC can be configured to produce a left channel, right channel, or (left + right)/2 output from the stereo input data. The IC also features an extremely robust digital audio interface with very high wideband jitter tolerance (12ns typ) on PDM_CLK. Active emissions-limiting, edge-rate limiting, and overshoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices and reduces the component count of the solution. The IC is available in a 9-pin WLP package (1.345mm x 1.435mm x 0.64mm) and is specified over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	PDM Input Class D Audio Power Amplifier
B. Process:	S18
C. Number of Device Transistors:	168605
D. Fabrication Location:	USA and Japan
E. Assembly Location:	USA
F. Date of Initial Production:	June 7, 2012

III. Packaging Information

A. Package Type:	9-bump WLP 3x3 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-4636
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	73°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	57.874X54.3307 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.06 @ 25°C and 1.05 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EAFL8Q002A, D/C 1221)

The AX54-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX98356EWL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	EAFL8Q002A, D/C 1221

Note 1: Life Test Data may represent plastic DIP qualification lots.