RELIABILITY REPORT

FOR

MAX98355AEWL+T

WAFER LEVEL PRODUCTS

January 29, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX98355AEWL+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
.....Attachments
IV. .....Die Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation

I. Device Description

A. General

The MAX98355A/MAX98355B are digital pulse-code modulation (PCM) input Class D power amplifiers that provide Class AB audio performance with Class D efficiency. These ICs offer five selectable gain settings (3dB, 6dB, 9dB, 12dB, and 15dB) set by a single gain-select input (GAIN). The digital audio interface is highly flexible with the MAX98355A supporting I²S data and the MAX98355B supporting left-justified data. Both ICs support time division multiplexed (TDM) data. The digital audio interface accepts sample rates ranging from 8kHz to 96kHz for all supported data formats. The ICs can be configured to produce a left channel, right channel, or (left + right)/2 output from the stereo input data. The ICs operate using 16/24/32-bit data for I²S and left justified modes as well as 16-bit data with up to four slots when using TDM mode. The ICs eliminate the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin count of the ICs. The ICs also feature a very high wideband jitter tolerance (12ns typ) on BCLK and LRCLK to provide robust operation. Active emissions-limiting, edge-rate limiting, and overshoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices and reduces the component count of the solution. The ICs are available in a 9-pin WLP package (1.345mm x 1.435mm x 0.64mm) and are specified over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	PCM Input Class D Audio Power Amplifiers
B. Process:	S18
C. Number of Device Transistors:	168605
D. Fabrication Location:	California
E. Assembly Location:	Texas
F. Date of Initial Production:	June 7, 2012

III. Packaging Information

A. Package Type:	9 bmp WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	
G. Assembly Diagram:	#05-9000-4636
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	73°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	57.874X54.3307 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135¿C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EAFL8Q002A D/C 1221)

The AX54-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX98355AEWL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	EAFL8Q002A, D/C 1221

Note 1: Life Test Data may represent plastic DIP qualification lots.