RELIABILITY REPORT

FOR

MAX98308EWC+

WAFER LEVEL PRODUCTS

April 13, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX98308EWC+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX98307/MAX98308 fully differential mono Class DG multilevel power amplifiers with integrated inverting charge pumps offer highly efficient, high-power audio solutions for portable applications. Class DG multilevel modulation extends the dynamic range of the output signal by employing a charge-pump-generated negative rail as needed to extend the supply voltage. This scheme results in high efficiency over a wide output power range. The ICs combine Maxim's active emissions limiting edge rate and overshoot control circuitry with multilevel output modulation to greatly reduce EMI. These features eliminate the need for output filtering as compared to traditional Class D devices, reducing component count and cost. The MAX98307's 16-pin TQFN package features an adjustable gain set by external resistors. The MAX98308's space-saving 12-bump WLP package features an internally fixed gain of 8.5dB, 11.5dB, 14.5dB, 17.5dB, and 20.5dB set by a single gain input. Both devices operate over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	3.3W Mono Class DG Multilevel Audio Amplifier
B. Process:	S18
C. Number of Device Transistors:	7839
D. Fabrication Location:	California
E. Assembly Location:	Texas
F. Date of Initial Production:	October 4, 2011

III. Packaging Information

A. Package Type:	12 bmp WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-4427
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	73°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	51.97X68.11 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{231 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.4 \times 10^{-9}$

$\lambda = 11.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot S0GZCQ001C, D/C 1120)

The AX53 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX98308EWC+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 231 hrs.	DC Parameters & functionality	80	0	S0GYCQ001A, D/C 1120

Note 1: Life Test Data may represent plastic DIP qualification lots.