RELIABILITY REPORT

FOR

MAX9669ETI+

PLASTIC ENCAPSULATED DEVICES

May 4, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX9669ETI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9669 outputs 16 voltage references for gamma correction in TFT LCDs and one voltage reference for VCOM. Each gamma reference voltage has its own 10-bit digital-to-analog converter (DAC) and buffer to ensure a stable voltage. The VCOM reference voltage has its own 10-bit DAC and an amplifier to ensure a stable voltage when critical levels and patterns are displayed. The MAX9669 features integrated multiple-time programmable (MTP) memory to store gamma and VCOM values on the chip, eliminating the need for external EEPROM. The MAX9669 supports up to 100 write operations to the on-chip nonvolatile memory. The gamma outputs can drive 250mA peak transient current and settle within 1Î¼s. The VCOM output can provide 400mA peak transient current and also settles within 1µs. The analog supply voltage range extends from 9V to 20V, and the digital supply voltage range extends from 2.7V to 3.6V. Gamma values and the VCOM value are programmed into registers through the I2C interface.

II. Manufacturing Information

A. Description/Function:	10-Bit Programmable Gamma Reference System with MTP for TFT LCDs
B. Process:	S45S
C. Number of Device Transistors:	4548
D. Fabrication Location:	Texas
E. Assembly Location:	UTL Thailand
F. Date of Initial Production:	January 19, 2009

III. Packaging Information

A. Package Type:	28-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	1.7°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	1.7°C/W

IV. Die Information

A. Dimensions:	99 X 101 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{54780 \times 4340 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV
And 54780 are number of device hours, 77*192 + 80*500)

$\lambda = 3.8 \times 10^{-9}$

$\lambda = 3.8$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S45 Process results in a FIT Rate of 0.9 @ 25C and 13.84 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The DV19 die type has been found to have all pins able to withstand a transient pulse of

HBM ESD: +/-2000 V per JEDEC JESD22-A114.
HBM CDM: +/-750 V per JEDEC JESD22-C101
HBM MM: +/-250 V per JEDEC JESD22-A115

Latch-Up testing has shown that this device withstands a current of +/-100 mA, 1.5x VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX9669ETI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	157	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0
Program (Note 3) **Erase** **Endurance Cycling** Package Level :	+25°C 100x	DC Parameters & functionality	160	0
Followed by:				
Data Retention Bake Package Level	150°C 1000 hrs	Read Back Data Only	80	0
High Temp Operating Life Package Level	135°C 1000 hrs	Read Back Data Only	80	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: P/E Endurance is performed prior to subjecting wafers for bake.