

RELIABILITY REPORT FOR

MAX9648AUK+T

PLASTIC ENCAPSULATED DEVICES

June 10, 2015

# **MAXIM INTEGRATED**

160 RIO ROBLES SAN JOSE, CA 95134

Approved by				
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Quality Assurance				
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#### Conclusion

The MAX9648AUK+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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# I. Device Description

A. General

The MAX9647/MAX9648 comparators are drop-in, pin-for-pin compatible replacements for the LMX331/LMX331H. The MAX9648 has the added benefit of internal hysteresis to provide noise immunity, preventing output oscillations even with slow moving input signals. Advantage of the ICs include low supply voltage, small package, and low cost. They also offer a wide supply voltage range, wide operating temperature range, competitive CMRR and PSRR, response time characteristics, input offset, low noise, output saturation voltage, input bias current and RF immunity. The ICs are available in both 5-pin SC70 and SOT23 packages.



#### II. Manufacturing Information

A. Description/Function: General-Purpose, Low-Voltage, Single Comparators in Tiny Packages

B. Process: S18C. Number of Device Transistors: 101D. Fabrication Location: California

E. Assembly Location: Malaysia, ThailandF. Date of Initial Production: September 13, 2011

# III. Packaging Information

A. Package Type: 5-pin SOT23
B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-9000-4620
H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

Level 1

J. Single Layer Theta Ja: 324.3°C/W
K. Single Layer Theta Jc: 82°C/W
L. Multi Layer Theta Ja: 255.9°C/W
M. Multi Layer Theta Jc: 81°C/W

### IV. Die Information

A. Dimensions: 16.93X22.05 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al with Ti/TiN Barrier

D. Backside Metallization: NoneE. Minimum Metal Width: 0.18umF. Minimum Metal Spacing: 0.18um

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO<sub>2</sub>I. Die Separation Method: Wafer Saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm</li>D. Sampling Plan: Mil-Std-105D

# VI. Reliability Evaluation

#### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate  $(\lambda)$  is calculated as follows:

$$x_{\rm h} = 2.67 \times 10^{-9}$$
  
 $x_{\rm h} = 2.67 \text{ F.I.T.} (60\% \text{ confidence level @ 25°C)}$ 

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

# B. E.S.D. and Latch-Up Testing (lot S24XYQ001B, D/C 1128)

The CM96-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78..



# **Table 1**Reliability Evaluation Test Results

# MAX9648AUK+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (No	ote 1)  Ta = 135°C  Biased  Time = 1000 hrs.	DC Parameters & functionality	79	0	S24XXQ001B, 1122

Note 1: Life Test Data may represent plastic DIP qualification lots.