RELIABILITY REPORT

FOR

MAX9647AUK+T / MAX9647AXK+T

PLASTIC ENCAPSULATED DEVICES

October 15, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX9647AUK+T / MAX9647AXK+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9647/MAX9648 comparators are drop-in, pin-for-pin compatible replacements for the LMX331/LMX331H. The MAX9648 has the added benefit of internal hysteresis to provide noise immunity, preventing output oscillations even with slow moving input signals.

Advantage of the ICs include low supply voltage, small package, and low cost. They also offer a wide supply voltage range, wide operating temperature range, competitive CMRR and PSRR, response time characteristics, input offset, low noise, output saturation voltage, input bias current and RF immunity. The ICs are available in both 5-pin SC70 and SOT23 packages.

II. Manufacturing Information

A. Description/Function:	General-Purpose, Low-Voltage, Single Comparators in Tiny Packages	
B. Process:	S18	
C. Number of Device Transistors:	101	
D. Fabrication Location:	USA	
E. Assembly Location:	Malaysia and Thailand	Malaysia and Thailand
F. Date of Initial Production:	September 13, 2011	

III. Packaging Information

A. Package Type:	5-pin SOT23	5-pin SC70
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4620	#05-9000-4621
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	324.3°C/W	324°C/W
K. Single Layer Theta Jc:	82°C/W	115°C/W
L. Multi Layer Theta Ja:	255.9°C/W	324°C/W
M. Multi Layer Theta Jc:	82°C/W	115°C/W

IV. Die Information

A. Dimensions:	16.93 X 22.05 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 2.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.06 @ 25C and 1.05 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot S24XXQ001B, D/C 1122)

The CM96-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX9647AUK+T / MAX9647AXK+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	S24XXQ001B, D/C 1122

Note 1: Life Test Data may represent plastic DIP qualification lots.