RELIABILITY REPORT

FOR

MAX9632ATA+T / MAX9632ASA+T

PLASTIC ENCAPSULATED DEVICES

July 30, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Operations

Conclusion

The MAX9632ATA+T / MAX9632ASA+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9632 is a low-noise, precision, wide-band operational amplifier that can operate in a very wide +4.5V to +36V supply voltage range. The IC operates in dual (±18V) or single-supply mode (36V). The exceptionally fast settling time and low distortion make the IC an excellent solution for precision acquisition systems. The rail-to-rail output swing maximizes the dynamic range when driving high-resolution 24-bit ADCs even with low supply voltages. The IC achieves 55MHz of gain-bandwidth product and ultra-low 0.94nV/ input voltage noise with only 3.9mA of quiescent current. The IC is offered in 8-pin SO and TDFN packages and is rated for operation over the -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	36V, Precision, Low-Noise, Wide-Band Amplifier
B. Process:	BiCMOS
C. Number of Device Transistors:	2026
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia and Thailand
F. Date of Initial Production:	September 22, 2010

III. Packaging Information

A. Package Type:	8-pin TDFN 3x3	8-pin SOIC (N)
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4022	#05-9000-4023
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	55°C/W	170°C/W
K. Single Layer Theta Jc:	8.3°C/W	40°C/W
L. Multi Layer Theta Ja:	42°C/W	136°C/W
M. Multi Layer Theta Jc:	8.3°C/W	38°C/W

IV. Die Information

A. Dimensions:	51.97X64.17 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier xxxx
D. Backside Metallization:	None?
E. Minimum Metal Width:	Metal1 = 0.6 / Metal2 = 0.6 / Metal3 = 4.0 microns (as drawn)xxxx
F. Minimum Metal Spacing:	Metal1 = 0.4 / Metal2 = 0.4 / Metal3 = 4.0 microns (as drawn)xxxx
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Operations) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the Process results in a FIT Rate of @ 25°C and @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot JG7ZB3011B, D/C 1104)

The OY48 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 8000V per JEDEC JESD22-A114
ESD-CDM: +/- 1000V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX9632ATA+T / MAX9632ASA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	JG7ZBA004B, D/C 1007

Note 1: Life Test Data may represent plastic DIP qualification lots.