RELIABILITY REPORT

FOR

MAX9600EUP+

PLASTIC ENCAPSULATED DEVICES

December 14, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX9600EUP+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9600/MAX9601/MAX9602 ultra-high-speed comparators feature extremely low propagation delay (500ps). These dual and quad comparators minimize propagation delay skew (10ps) and are designed for low propagation delay dispersion (30ps). These features make them ideal for applications where high-fidelity tracking of narrow pulses and low timing dispersion is critical. The differential input stage accepts a wide range of signals in the common-mode range from (VEE + 3V) to (VCC - 2V). The outputs are complementary digital signals, compatible with ECL and PECL systems, and provide sufficient current to directly drive transmission lines terminated in 50 . The MAX9600/MAX9601 dual-channel ECL and dual-channel PECL output comparators incorporate latch enable (LE_, active-low LE_), and hysteresis (HYS_). The complementary latch-enable control permits tracking, track-hold or sample-hold mode of operations. The latch-enables can be driven with standard ECL logic for MAX9600 and PECL logic for MAX9601. The MAX9602 quad-channel PECL output comparator is ideal for high-density packaging in limited board space. The MAX9600/MAX9601 are available in 20-pin TSSOP packages, and the MAX9602 is offered in a 24-pin TSSOP package. The MAX9600/MAX9601/MAX9602 are specified for operation from -40°C to +85°C.

II. Manufacturing Information

A. Description/Function:	Dual ECL and Dual/Quad PECL, 500ps, Ultra-High-Speed Comparators
B. Process:	GST20
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Thailand
F. Date of Initial Production:	October 8, 2002

III. Packaging Information

A. Package Type:	20L TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1501-0267 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	91°C/W
K. Single Layer Theta Jc:	20°C/W
L. Multi Layer Theta Ja:	73.8°C/W
M. Multi Layer Theta Jc:	20°C/W

IV. Die Information

A. Dimensions:	61 X 65 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 24.4 \times 10^{-9}$

$\lambda = 24.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the GST20 Process results in a FIT Rate of 0.06 @ 25C and 1.10 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NC40BQ002B D/C 0232)

The CM75 die type has been found to have all pins able to withstand a HBM transient pulse of +/-400V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX9600EUP+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0	NC40BQ002B, D/C 0232

Note 1: Life Test Data may represent plastic DIP qualification lots.