RELIABILITY REPORT

FOR

MAX951ExA

PLASTIC ENCAPSULATED DEVICES

June 26, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX951 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description

II.Manufacturing Information

III.Packaging Information

IV.Die Information

V.Quality Assurance Information

VI.Reliability Evaluation

IV.Attachments

I. Device Description

A. General

The MAX951 features combinations of a micropower operational amplifier, comparator, and reference in an 8-pin package. In the MAX951 the comparator's inverting input is connected to an internal 1.2V \pm 2% bandgap reference. The MAX951 operates from a single \pm 2.7V to \pm 7V supply with a typical supply current of \mp 7µA. Both the op amp and comparator feature a common-mode input voltage range that extends from the negative supply rail to within 1.6V of the positive rail, as well as output stages that swing rail to rail.

The op amps in the MAX951 are internally compensated to be unity-gain stable. This op amp has a unique output stage that enables it to operate with an ultra-low supply current while maintaining linearity under loaded conditions. In addition, it has been designed to exhibit good DC characteristics over their entire operating temperature range, minimizing input referred errors.

The comparator output stage of this device continuously sources as much as 40mA. The comparator eliminates power-supply glitches that commonly occur when changing logic states, minimizing parasitic feedback and making this device easier to use. In addition, it contains ± 3 mV internal hysteresis to ensure clean output switching, even with slow-moving input signals.

B. Absolute Maximum Ratings

<u>ltem</u>	<u>Rating</u>
Supply Voltage (V _{DD} to V _{SS})	9V
Inputs	
Current (AMPIN_, COMPIN_)	20mA
Voltage (AMPIN_, COMPIN_)	$(V_{DD} + 0.3V)$ to $(V_{SS} - 0.3V)$
Outputs	
Current (AMPOUT, COMPOUT)	50mA
Current (REF)	20mA
Voltage (AMPOUT, COMPOUT, REF)	$(V_{DD} + 0.3V)$ to $(V_{SS} - 0.3V)$
Short-Circuit Duration (REF, AMPOUT)	Continuous
Short-Circuit Duration (COMPOUT, V_{DD} to $V_{SS} \le 7V$)	1min
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin PDIP	727mW
8-Pin NSO	471mW
8-Pin uMAX	330mW
Derates above +70°C	
8-Pin PDIP	9.09mW/°C
8-Pin NSO	5.88mW/°C
8-Pin uMAX	4.1mW/°C

II. Manufacturing Information

A. Description/Function: Ultra-Low-Power, Single-Supply Op Amp + Comparator + Reference

B. Process: S3 - Standard 3 micron silicon gate CMOS

C. Number of Device Transistors: 163

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malaysia, or Thailand

F. Date of Initial Production: September, 1995

III. Packaging Information

A. Package Type:	8-Lead NSO	8-Lead PDIP	8-Lead uMAX
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0601-0414	# 05-0601-0415	# 05-0601-0416
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions: 58x84 mils

B. Passivation: SiN/SiO (nitride/oxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 3 microns (as drawn)

F. Minimum Metal Spacing: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \text{ x } 4389 \text{ x } 560 \text{ x } 2} \text{ (Chi square value for MTTF upper limit)}$$

$$\text{Temperature Acceleration factor assuming an activation energy of } 0.8eV$$

$$\lambda = 1.94 \text{ x } 10^{-9}$$

$$\lambda = 1.94 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5066) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OA64-1 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1 Reliability Evaluation Test Results

MAX951ExA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION		SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	(Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		560	0
Moisture Testin	g (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP NSO uMAX	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stre	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

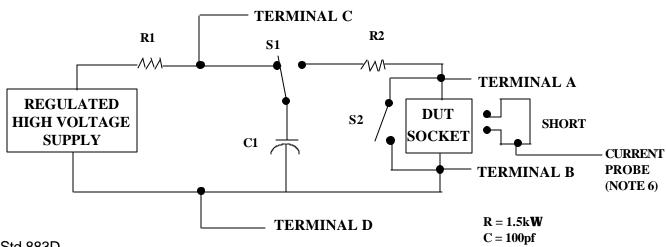
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2}$ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

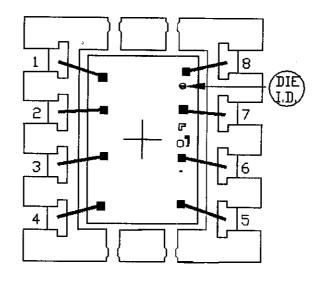
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

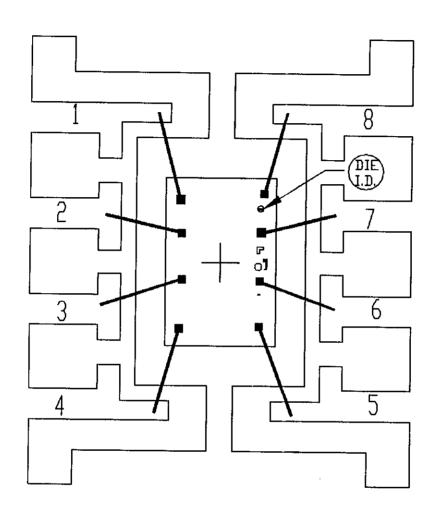
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \(\lambda_{S1} \), or \(\lambda_{S2} \) or \(\lambda_{S3} \) or \(\lambda_{CC1} \), or \(\lambda_{CC2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8



PKG.CODE: U8-1		APPROVALS	DATE	NIXIXI	1/1
CAV./PAD SIZE:	PKG.		•	BUILDSHEET NUMBER	REV.
68X94	DESIGN	•		05-0601-0416	В



PKG.CODE: S8-4		APPROVALS	DATE	NIXIN	7 1
CAV./PAD SIZE:	PKG.				REV.
90 X 130	DESIGN			05-0601-0415	В

