

RELIABILITY REPORT
FOR
MAX942CPA+
PLASTIC ENCAPSULATED DEVICES

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# **MAXIM INTEGRATED**

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#### Conclusion

The MAX942CPA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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# I. Device Description

A. General

The MAX941/MAX942/MAX944 are single/dual/quad high-speed comparators optimized for systems powered from a 3V or 5V supply. These devices combine high speed, low power, and rail-to-rail inputs. Propagation delay is 80ns, while supply current is only 350µA per comparator. The input common-mode range of the MAX941/MAX942/MAX944 extends beyond both power-supply rails. The outputs pull to within 0.4V of either supply rail without external pullup circuitry, making these devices ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals. The MAX941 features latch enable and device shutdown. The single MAX941 and dual MAX942 are offered in a tiny µMAX® package. Both the single and dual MAX942 are available in 8-pin DIP and SO packages. The quad MAX944 comes in 14-pin DIP and narrow SO packages.



#### II. Manufacturing Information

A. Description/Function: High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

B. Process: CB3

C. Number of Device Transistors:

D. Fabrication Location: Oregon

E. Assembly Location: Thailand, Philippines, Malaysia

F. Date of Initial Production: Pre 1997

# III. Packaging Information

A. Package Type: 8-pin PDIP
B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-1501-0239
H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

Level 1

J. Single Layer Theta Ja: 110°C/W
K. Single Layer Theta Jc: 40°C/W
L. Multi Layer Theta Ja: N/A
M. Multi Layer Theta Jc: N/A

### IV. Die Information

A. Dimensions: 76X24 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub> (Silicon nitride)

C. Interconnect: Au

D. Backside Metallization: None

E. Minimum Metal Width: Metal1 = 0.5 microns (as drawn)
 F. Minimum Metal Spacing: Metal1 = 0.45 microns (as drawn)

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO<sub>2</sub>I. Die Separation Method: Wafer Saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm</li>D. Sampling Plan: Mil-Std-105D

# VI. Reliability Evaluation

#### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate  $(\lambda)$  is calculated as follows:

$$\lambda = 1 \over MTTF$$
 =  $\frac{1.83}{192 \times 4340 \times 320 \times 2}$  (Chi square value for MTTF upper limit)  $\frac{1}{192 \times 4340 \times 320 \times 2}$  (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 3.44 \times 10^{-9}$$
  
 $\lambda = 3.44 \text{ F.I.T. (60\% confidence level @ 25°C)}$ 

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the CB3 Process results in a FIT Rate of 0.09 @ 25C and 1.49 @ 55C (0.8 eV, 60% UCL)

# B. E.S.D. and Latch-Up Testing (ESD lot HCJAEX001Q D/C 9706, Latch-Up lot HCJAEA012A D/C 9803)

The CM69-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.



# **Table 1**Reliability Evaluation Test Results

# MAX942CPA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (	Note 1)				
	Ta = 135°C	DC Parameters	80	0	HCJAEX001Q, D/C 9706
	Biased	& functionality	80	0	VCJADX002A, D/C NA
	Time = 192 hrs.		80	0	VCJABX003C, D/C NA
			80	0	VCJAAX001B, D/C 9401

Note 1: Life Test Data may represent plastic DIP qualification lots.