RELIABILITY REPORT

FOR

MAX9282GTM+T

PLASTIC ENCAPSULATED DEVICES

February 17, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX9282GTM+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9278/MAX9282 gigabit multimedia serial link (GMSL) deserializers receive data from a GMSL serializer over 50 coax or 100 shielded twisted-pair (STP) cable and output deserialized data on 3 of 4 data-lane LVDS outputs (oLDI). The MAX9282 has HDCP content protection but otherwise is the same as the MAX9278. The deserializers pair with any GMSL serializer capable of coax output. When programmed for STP input, they are backward compatible with any GMSL serializer. The audio channel supports L-PCM I2S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits. The embedded control channel operates at 9.6kbps to 1Mbps in UART-to-UART and UART-to-I2C modes, and up to 1Mbps in I2C-to-I2C mode. Using the control channel, a µC can program serializer, deserializer, and peripheral device registers at any time, independent of video timing, and manage HDCP operation (MAX9282). Two GPIO ports are included, allowing display power-up and switching of the backlight among other uses. A continuously sampled GPI input supports touch-screen controller interrupt requests in display applications. For use with longer cables, the deserializers have a programmable cable equalizer. Programmable spread spectrum is available on the LVDS output. The serial input and LVDS output meet ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 3.0V to 3.6V and the I/O supply is 1.7V to 3.6V. The devices are in lead-free, 48-pin, 7mm × 7mm TQFN and QFND packages with exposed pad and 0.5mm lead pitch.

II. Manufacturing Information

A. Description/Function:	3.12Gbps GMSL Deserializers for Coax or STP Input and LVDS Output
B. Process:	TS18
C. Number of Device Transistors:	1122155
D. Fabrication Location:	Taiwan
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	February 10, 2014

III. Packaging Information

A. Package Type:	48-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5464
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	166.1417 X 173.622 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.1 @ 25°C and 1.9 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QAUL8A004AA, D/C 1429)

The HS66-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX9282GTM+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	QANQ2Q003BD, D/C 1408

Note 1: Life Test Data may represent plastic DIP qualification lots.