

RELIABILITY REPORT FOR MAX9272GTM+T

PLASTIC ENCAPSULATED DEVICES

September 25, 2013

MAXIM INTEGRATED

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Approved by			
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Conclusion

The MAX9272GTM+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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- I. Device Description
 - A. General

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The MAX9272 compact deserializer is designed to interface with a GMSL serializer over 50 coax or 100 shielded twisted-pair (STP) cable. The device pairs with the MAX9271 or MAX9273 serializers. The parallel output is programmable for single or double output. Double output strobes out half of a parallel word on each pixel clock cycle. Double output can be used with GMSL serializers that have the double-input feature. The device features an embedded control channel that operates at 9.6kbps to 1Mbps in UART and mixed UART/I²C modes, and up to 400kbps in I²C mode. Using the control channel, a microcontroller (μ C) is capable of programming serializer/deserializer and peripheral device registers at any time, independent of video timing. Two GPIO ports are included, allowing power-up and switching of the backlight in display applications and similar uses. A continuously sampled GPI input supports touch-screen controller interrupt requests. For use with longer cables, the device has a programmable equalizer. Programmable spread spectrum is available on the parallel output. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply range is 1.7V to 1.9V and the I/O supply range is 1.7V to 3.6V. The device is available in a 48-pin (7mm × 7mm) TQFN-EP package with 0.5mm lead pitch and operates over the -40°C to +105°C temperature range.



28-Bit GMSL Deserializer for Coax or STP Cable

TS18

370041

Taiwan

China, Taiwan and Thailand

II. Manufacturing Information

- A. Description/Function:
- B. Process:
- C. Number of Device Transistors:
- D. Fabrication Location:
- E. Assembly Location:
- F. Date of Initial Production: June 29, 2012

III. Packaging Information

Α.	Package Type:	48-pin TQFN 7x7
В.	Lead Frame:	Copper
C.	Lead Finish:	100% matte Tin
D.	Die Attach:	Conductive
E.	Bondwire:	Au (0.8 mil dia.)
F.	Mold Material:	Epoxy with silica filler
G.	Assembly Diagram:	#05-9000-4832
Н.	Flammability Rating:	Class UL94-V0
I.	Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J.	Single Layer Theta Ja:	36°C/W
K.	Single Layer Theta Jc:	1°C/W
L.	Multi Layer Theta Ja:	25°C/W
M.	Multi Layer Theta Jc:	1°C/W

IV. Die Information

Α.	Dimensions:	125.985 X 125.985 mils
В.	Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C.	Interconnect:	Al/0.5%Cu
D.	Backside Metallization:	None
E.	Minimum Metal Width:	0.23 microns (as drawn)
F.	Minimum Metal Spacing:	0.23 microns (as drawn)
G.	Bondpad Dimensions:	
Н.	Isolation Dielectric:	SiO ₂
I.	Die Separation Method:	Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)	
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.	
C. Observed Outgoing Defect Rate:	< 50 ppm	
D. Sampling Plan:	Mil-Std-105D	

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\mathcal{R} = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 78 \times 2}$$
(Chi square value for MTTF upper limit)
where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 14.1 \times 10^{-9}$$

 λ = 14.1 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.05 @ 25°C and 0.86 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The HS50-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114 (lot QAFZ5Q002D, D/C 1307)
ESD-CDM:	+/- 750V per JEDEC JESD22-C101 (lot QAFZ5Q002D, D/C 1307)
ESD-MM:	+/- 200V per JEDEC JESD22-A115 (lot QAFZ5Q002D, D/C 1307)

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78 (lot QAFZ5Q001B, D/C 1216).



Table 1 Reliability Evaluation Test Results

MAX9272GTM+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note	1) Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	78	0	QAFZ5Q001B, D/C 1216

Note 1: Life Test Data may represent plastic DIP qualification lots.