RELIABILITY REPORT

FOR

MAX9209EUM+

PLASTIC ENCAPSULATED DEVICES

October 26, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX9209EUM+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9209/MAX9213 serialize 21 bits of LVTTL/LVCMOS parallel input data to three LVDS outputs. A parallel rate clock on a fourth LVDS output provides timing for deserialization. The MAX9209/MAX9213 feature programmable DC balance, which allows isolation between the serializer and deserializer using AC-coupling. The DC balance circuits on each channel code the data, limiting the imbalance of transmitted ones and zeros to a defined range. The companion MAX9210/MAX9214 deserializers decode the data. When DC balance is not programmed, the serializers are compatible with non-DC-balanced, 21-bit serializers such as the DS90CR215 and DS90CR217. Two frequency ranges and two DC-balance default conditions are available for maximum replacement flexibility and compatibility with existing non-DC-balanced serializers. The MAX9209/MAX9213 are available in TSSOP and space-saving thin QFN packages.

II. Manufacturing Information

A. Description/Function:	Programmable DC-Balanced 21-Bit Serializers
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines, Malaysia
F. Date of Initial Production:	July 25, 2003

III. Packaging Information

A. Package Type:	48-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0468
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	62.4°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	88 X 117 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 224 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 0.9 \times 10^{-9}$

λ = 0.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (Lot QFE0AA048A D/C 1022)

The HS30 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX9209EUM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	45	0	QFE0AQ003B, D/C 0451
	Biased	& functionality	45	0	QFE2AQ001B, D/C 0304
	Time = 1000 hrs.		45	0	QFE2AQ001C, D/C 0304
			44	0	QFE2AQ001E, D/C 0304
			45	0	QFE2AQ001Q, D/C 0404

Note 1: Life Test Data may represent plastic DIP qualification lots.