MAX9206EAI Rev. B

RELIABILITY REPORT

FOR

MAX9206EAI

PLASTIC ENCAPSULATED DEVICES

August 15, 2004

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX9206 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9206 deserializer transforms a high-speed serial bus low-voltage differential signaling (BLVDS) data stream into 10bit-wide parallel LVCMOS/ LVTTL data and clock. The deserializer pairs with a serializer such as the MAX9205, which generates a serial BLVDS signal from 10-bit-wide parallel data. The serializer/deserializer combination reduces interconnect, simplifies PC board layout, and reduces board size.

The MAX9206 receives serial data at 400Mbps over board traces or twisted-pair cables. This device combines frequency lock, bit lock, and frame lock to produce a parallel-rate clock and word-aligned 10-bit data. Serialization eliminates parallel bus clock-to-data and data-to-data skew.

A power-down mode reduces typical supply current to less than 600µA. Upon power-up (applying power or driving PWRDNbar high), the MAX9206 establishes lock after receiving synchronization signals or serial data from the MAX9205. An output enable allows the outputs to be disabled, putting the parallel data outputs and recovered output clock into a high-impedance state without losing lock.

The MAX9206 operates from a single +3.3V supply and are specified for operation from -40°C to +85°C. The MAX9206 is available in a 28-pin SSOP packages.

| B. Absolute Maximum Ratings | |
|---|----------------------|
| ltem | Rating |
| | |
| AVCC, DVCC to AGND, DGND | -0.3V to +4V |
| RI+, RI- to AGND, DGND | -0.3V to +4V |
| All Other Pins to DGND | -0.3V to DVCC + 0.3V |
| ROUT_ Short-Circuit Duration (Note 1) | Continuous |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| ESD Rating (Human Body Model, RI+, RI-) | ±8kV |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 28-Pin SSOP | 762mW |
| Derates above +70°C | |
| 28-Pin SSOP | 9.5mW/°C |

II. Manufacturing Information

| A. Description/Function: | 10-Bit Bus LVDS Deserializer |
|----------------------------------|------------------------------|
| B. Process: | TC35 |
| C. Number of Device Transistors: | 9602 |
| D. Fabrication Location: | Taiwan |
| E. Assembly Location: | Philippines or Malaysia |
| F. Date of Initial Production: | July, 2001 |

III. Packaging Information

| A. Package Type: | 28-Pin SSOP |
|---|--------------------------------|
| B. Lead Frame: | Copper |
| C. Lead Finish: | Solder Plate or 100% Matte Tin |
| D. Die Attach: | Silver-filled Epoxy |
| E. Bondwire: | Gold (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-2801-0023 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity | |

per JEDEC standard JESD22-112: Level 1

IV. Die Information

| A. Dimensions: | 75 x 93 mils |
|----------------------------|--|
| B. Passivation: | Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | M1 = 0.5 / M2 = 0.6 / M3 = 0.6 microns (as drawn) |
| F. Minimum Metal Spacing: | M1 = 0.45 / M2 = 0.5 / M3 = 0.6 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

| Α. | Quality Assurance Contacts: | Jim Pedicord (Manager, Reliability Operations) |
|----|-----------------------------|--|
| | | Bryan Preeshl (Managing Director) |

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{192 \text{ x } 4340 \text{ x } 80 \text{ x } 2}$ (Chi square value for MTTF upper limit) Temperature Acceleration factor assuming an activation energy of 0.8eV

 $\lambda = 13.74 \times 10^{-9}$

 λ = 13.74 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. #06-5836) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**).

Current monitor data for the TC35 Process results in a FIT Rate of 0.28 @ 25C and 4.76 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The HS06 die type has been found to have all pins able to withstand a transient pulse of \pm 1500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of \pm 250mA.

Table 1 Reliability Evaluation Test Results

MAX9206EAI

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|----------------------|---|----------------------------------|---------|----------------|-----------------------|
| Static Life Test | t (Note 1) | | | | |
| | Ta = 135°C Biased Time = 192 hrs. | DC Parameters & functionality | | 80 | 0 |
| Moisture Testi | ng (Note 2) | | | | |
| Pressure Pot | Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs. | DC Parameters & functionality | SSOP | 77 | 0 |
| 85/85 | Ta = 85°C RH = 85% Biased Time = 1000hrs. | DC Parameters & functionality | | 77 | 0 |
| Mechanical Str | ress (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters & functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

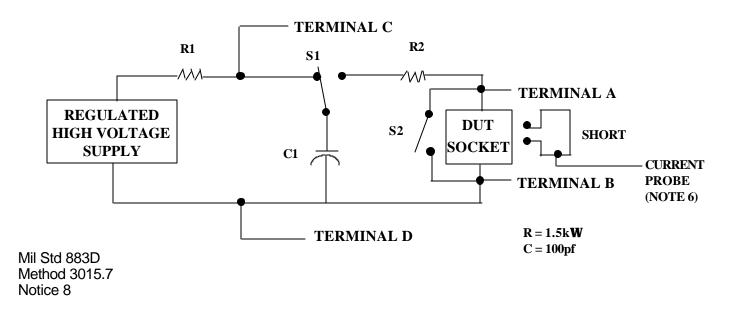
| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|----|---|---|
| 1. | All pins except V _{PS1} <u>3/</u> | All V_{PS1} pins |
| 2. | All input and output pins | All other input-output pins |

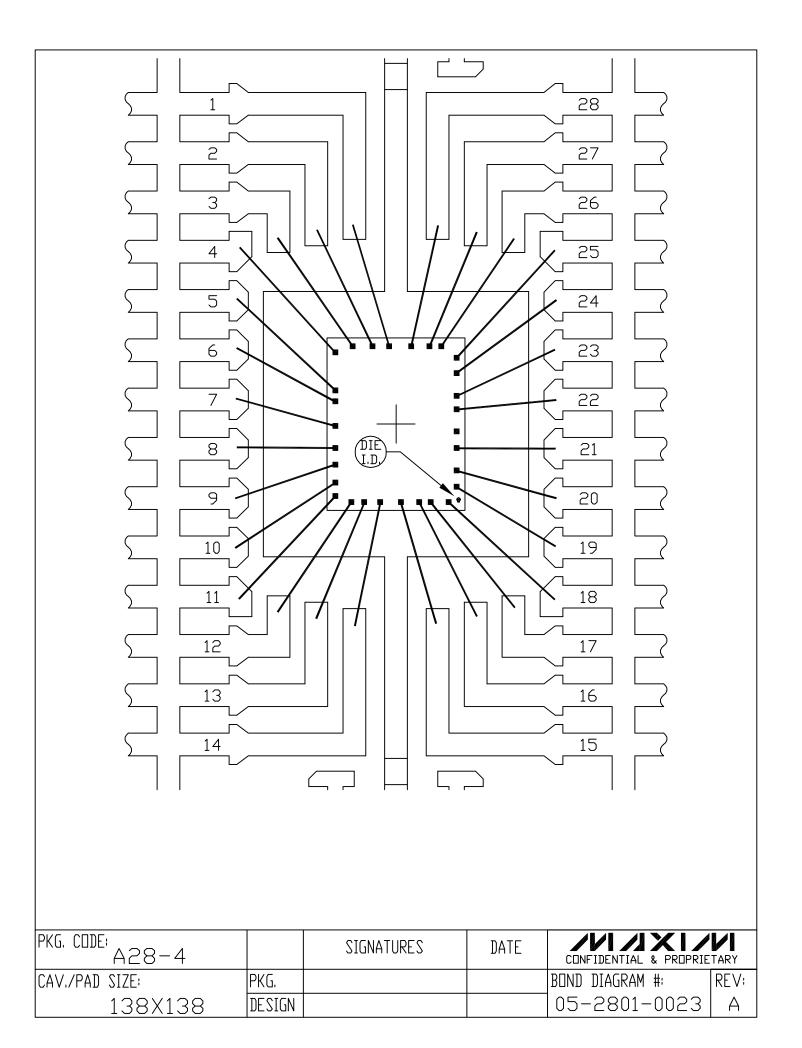
TABLE II. Pin combination to be tested. 1/2/

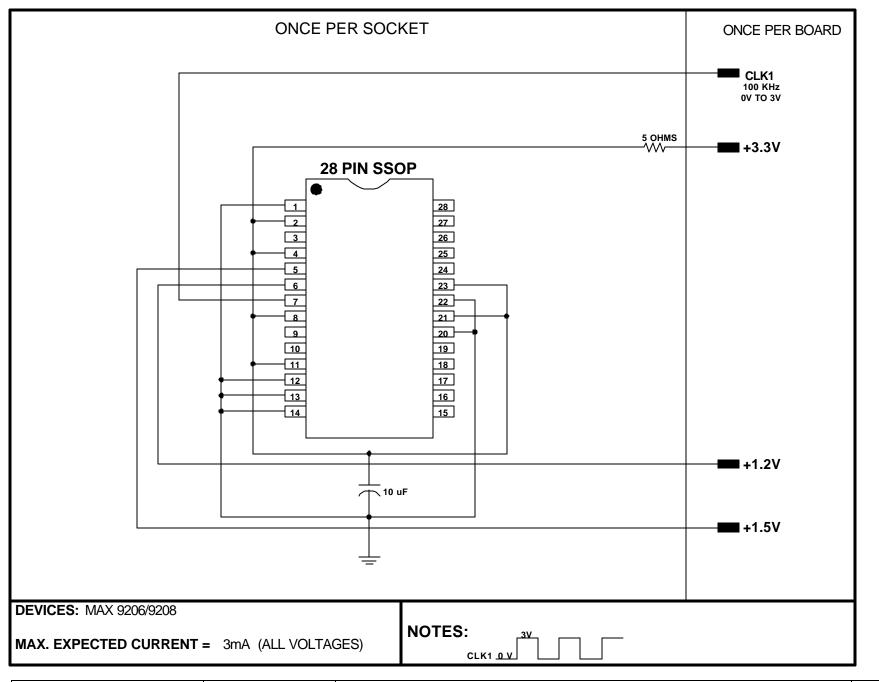
- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2/}$ No connects are not to be tested.
- $\overline{3/}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

- 3.4 <u>Pin combinations to be tested.</u>
 - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
 - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
 - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







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