



RELIABILITY REPORT  
FOR  
MAX918EUK+  
PLASTIC ENCAPSULATED DEVICES

October 13, 2010

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

|                                  |
|----------------------------------|
| <b>Approved by</b>               |
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| Quality Assurance                |
| Manager, Reliability Engineering |

## Conclusion

The MAX918EUK+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX917-MAX920 nanopower comparators in space-saving SOT23 packages feature Beyond-the-Rails(tm) inputs and are guaranteed to operate down to +1.8V. The MAX917/MAX918 feature an on-board  $1.245V \pm 1.5\%$  reference and draw an ultra-low supply current of only 750nA, while the MAX919/MAX920 (without reference) require just 380nA of supply current. These features make the MAX917-MAX920 family of comparators ideal for all 2-cell battery applications, including monitoring/management. The unique design of the output stage limits supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. This design also minimizes overall power consumption under dynamic conditions. The MAX917/MAX919 have a push-pull output stage that sinks and sources current. Large internal output drivers allow rail-to-rail output swing with loads up to 8mA. The MAX918/MAX920 have an open-drain output stage that makes them suitable for mixed-voltage system design.

## II. Manufacturing Information

|                                  |                                                                             |
|----------------------------------|-----------------------------------------------------------------------------|
| A. Description/Function:         | SOT23, 1.8V, Nanopower, Beyond-the-Rails Comparators With/Without Reference |
| B. Process:                      | S12                                                                         |
| C. Number of Device Transistors: |                                                                             |
| D. Fabrication Location:         | Oregon, California or Texas                                                 |
| E. Assembly Location:            | Malaysia, Philippines, Thailand                                             |
| F. Date of Initial Production:   | July 20, 1999                                                               |

## III. Packaging Information

|                                                                          |                          |
|--------------------------------------------------------------------------|--------------------------|
| A. Package Type:                                                         | 5-pin SOT23              |
| B. Lead Frame:                                                           | Copper                   |
| C. Lead Finish:                                                          | 100% matte Tin           |
| D. Die Attach:                                                           | Conductive               |
| E. Bondwire:                                                             | Au (1 mil dia.)          |
| F. Mold Material:                                                        | Epoxy with silica filler |
| G. Assembly Diagram:                                                     | #05-1501-0158            |
| H. Flammability Rating:                                                  | Class UL94-V0            |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1                  |
| J. Single Layer Theta Ja:                                                | 324.3°C/W                |
| K. Single Layer Theta Jc:                                                | 82°C/W                   |
| L. Multi Layer Theta Ja:                                                 | N/A                      |
| M. Multi Layer Theta Jc:                                                 | N/A                      |

## IV. Die Information

|                            |                                                                                     |
|----------------------------|-------------------------------------------------------------------------------------|
| A. Dimensions:             | 56 X 38 mils                                                                        |
| B. Passivation:            | Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide) |
| C. Interconnect:           | Al/0.5%Cu with Ti/TiN Barrier                                                       |
| D. Backside Metallization: | None                                                                                |
| E. Minimum Metal Width:    | 1.2 microns (as drawn)                                                              |
| F. Minimum Metal Spacing:  | 1.2 microns (as drawn)                                                              |
| G. Bondpad Dimensions:     | 5 mil. Sq.                                                                          |
| H. Isolation Dielectric:   | SiO <sub>2</sub>                                                                    |
| I. Die Separation Method:  | Wafer Saw                                                                           |

## V. Quality Assurance Information

|                                   |                                                                                                 |
|-----------------------------------|-------------------------------------------------------------------------------------------------|
| A. Quality Assurance Contacts:    | Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA)            |
| B. Outgoing Inspection Level:     | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm                                                                                        |
| D. Sampling Plan:                 | Mil-Std-105D                                                                                    |

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S12 Process results in a FIT Rate of 0.17 @ 25C and 3.00 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot I78BAQ001B, D/C 9923)

The CM44-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX918EUK+**

| TEST ITEM                        | TEST CONDITION                          | FAILURE IDENTIFICATION           | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS            |
|----------------------------------|-----------------------------------------|----------------------------------|-------------|--------------------|---------------------|
| <b>Static Life Test</b> (Note 1) | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 80          | 0                  | I78AAQ001C, DC 9923 |

Note 1: Life Test Data may represent plastic DIP qualification lots.