RELIABILITY REPORT

FOR MAX9175EUB+T

PLASTIC ENCAPSULATED DEVICES

January 26, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX9175EUB+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9174/MAX9175 are 670MHz, low-jitter, low-skew 1:2 splitters ideal for protection switching, loopback, and clock and signal distribution. The devices feature ultra-low 1.0ps(RMS) random jitter (max) that ensures reliable operation in high-speed links that are highly sensitive to timing errors. The MAX9174 has a fail-safe LVDS input and LVDS outputs. The MAX9175 has an anything differential input (CML/LVDS/LVPECL) and LVDS outputs. The outputs can be put into high impedance using the power-down inputs. The MAX9174 features a fail-safe circuit that drives the outputs high when the input is open, undriven and shorted, or undriven and terminated. The MAX9175 has a bias circuit that forces the outputs high when the input is open. The power-down inputs are compatible with standard LVTTL/LVCMOS logic. The power-down inputs tolerate undershoot of -1V and overshoot of VCC + 1V. The MAX9174/MAX9175 are available in 10-pin µMAX and 10-lead thin QFN with exposed pad packages, and operate from a single +3.3V supply over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	April 26, 2003

III. Packaging Information

A. Package Type:	10-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0517
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	180°C/W
K. Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	113.1°C/W
M. Multi Layer Theta Jc:	41.9°C/W

IV. Die Information

A. Dimensions:	57 X 71 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HS25-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA.

Table 1
Reliability Evaluation Test Results

MAX9175EUB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data