RELIABILITY REPORT

FOR

MAX9107

PLASTIC ENCAPSULATED DEVICES

February 19, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX9107 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9107/MAX9108/MAX9109dual/quad/single, high-speed, low-power voltage comparators are designed for use in systems powered from a single +5V supply. Their 25ns propagation delay (with 10mV input overdrive) is achieved with a power consumption of only 1.75mW per comparator. The wide input common- mode range extends from 200mV below ground to within 1.5V of the positive supply rail. The MAX9107/MAX9108/MAX9109 outputs are TTLcompatible, requiring no external pullup circuitry. These easy-to-use comparators incorporate internal hysteresis to ensure clean output switching even when the devices are driven by a slow-moving input signal. The MAX9107/MAX9108/MAX9109 are higher-speed, lower-power, lower-cost upgrades to industry-standard comparators MAX907/MAX908/MAX90T9h. The MAX9109 features an output latch but does not have complementary outputs. The dual MAX9107 is available in both 8-pin SO and SOT23 packages. The quad MAX9108 is available in 14-pin TSSOP and SO packages while the single MAX9109 is available in an ultra-small 6-pin SC70 package, a space-saving 6-pin SOT23 package and an 8-pin SO package.

II. Manufacturing Information

A. Description: Dual, High-Speed, Ultra-Low-Power, Single-Supply TTL Comparators

B. Process: CB3

C. Number of Device Transistors: 262

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia, Philippines or Thailand

F. Date of Initial Production: April 28, 2001

III. Packaging Information

A. Package Type: 8-Pin SOIC 8-Pin SO

B. Lead Frame: Copper Copper

C. Lead Finish: Solder Plate Solder Plate

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1.0 mil dia.) Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-1501-0256 Buildsheet # 05-1501-0254

H. Flammability Rating: Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-A112: Level 1 Level 1

IV. Die Information

A. Dimensions: 80 x 24 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Gold

D. Backside Metallization: None

E. Minimum Metal Width: Metal 1: 1.4 microns Metal 2: 1.4 microns Metal 3: 3 microns (as drawn)

F. Minimum Metal Spacing: Metal 1: 1.6 microns Metal 2: 1.6 microns Metal 3: 3 microns (as drawn)

G. Bondpad Dimensions: 2.7 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \underbrace{\frac{1}{\text{MTTF}}} = \underbrace{\frac{1.83}{192 \times 4389 \times 79 \times 2}}_{\text{Temperature Acceleration factor assuming an activation energy of 0.8eV}$$

$$\lambda = 13.75 \times 10^{-9}$$

$$\lambda = 13.75 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0002) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR- 1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The CM73 die type has been found to have all pins able to withstand a transient pulse of ± 2500 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1 Reliability Evaluation Test Results

MAX9107

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
		IDENTIFICATION	TAGRAGE	OIZL .	TAILOREO
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		79	0
Moisture Testir	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	DIP SO	77 77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, +V_S, -V_S, V_{REF}, etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \(\lambda_{S1} \), or \(\lambda_{S2} \) or \(\lambda_{S3} \) or \(\lambda_{C1} \), or \(\lambda_{C2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





