

RELIABILITY REPORT
FOR
MAX9092AKA+
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX9092AKA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9092/MAX9093/MAX9094/MAX9095 comparators are pin-for-pin compatible replacements for the LMX393/LMX393H/LMX339/LMX339H, respectively. The MAX9093/MAX9095 have the added benefit of internal hysteresis to provide noise immunity, preventing output oscillations even with slow-moving input signals. Advantages of the ICs include low supply voltage, small package, and low cost. They also offer a wide supply voltage range, wide operating temperature range, competitive CMRR and PSRR, response time characteristics, input offset, low noise, output saturation voltage, input bias current, and RF immunity. The ICs are available in both 8-pin SOT23/μMAX® and 14-pin TSSOP/SO packages.

II. Manufacturing Information

A. Description/Function:	General-Purpose, Low-Voltage, Dual/Quad, Tiny Pack Comparators
B. Process:	S18
C. Number of Device Transistors:	380
D. Fabrication Location:	California
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	June 29, 2012

III. Packaging Information

A. Package Type:	8-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4886
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Jb:	110°C/W
K. Single Layer Theta Jc:	80°C/W
L. Multi Layer Theta Ja:	196°C/W
M. Multi Layer Theta Jc:	70°C/W

IV. Die Information

A. Dimensions:	24.0157X50 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 2.6 \times 10^{-9}$$

$$\lambda = 2.6 \text{ F.I.T. (60\% confidence level @ 25 °C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93@ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SADX1Q001A, D/C 1207)

The CM97-2 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101
ESD-MM:	+/- 250V per JEDEC JESD22/A115

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX9092AKA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	80	0	SADU8Q001F, D/C 1207

Note 1: Life Test Data may represent plastic DIP qualification lots.