RELIABILITY REPORT

FOR

MAX9040xEUK

PLASTIC ENCAPSULATED DEVICES

September 3, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX9040 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9040 features a combination a of low-power comparators and a precision voltage reference. It's operating voltage range makes them ideal for both +3V and +5V systems. The MAX9040 has a single comparator and reference consuming only $40\mu A$ of supply current. Low-voltage operation and low supply current make these devices ideal for battery-operated systems.

The comparator features Rail-to-Rail® inputs and outputs, with a common-mode input voltage range that extends 250mV beyond the supply rails. Input bias current is typically 1.0pA, and input offset voltage is typically 0.5mV. Internal hysteresis ensures clean output switching, even with slow-moving input signals. The output stage features a unique design that limits supply current surges while switching, virtually eliminating supply glitches typical of many other comparators. This design also minimizes overall power consumption under dynamic conditions. The comparator outputs have rail-to-rail push-pull output stages that sink and source up to 8mA. The propagation delay is 400ns, even with the low operating supply current.

The reference output voltage is set to 2.048V in the MAX9040. These devices are offered in two grades: an A grade with 0.4% initial accuracy and 6ppm/°C tempco, and a B grade with 1% initial accuracy and 100ppm/°C tempco. The voltage reference features a proprietary curvature-correction circuit and laser-trimmed thin-film resistors. The series-mode references can sink or source up to 500µA of load current

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B. Absolute Maximum Ratings

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<u>item</u>	Kaung
Supply Voltage (VCC to VEE) All other pins Junction Temperature Storage Temp.	-0.3V to +6V (VEE - 0.3V) to (VCC + 0.3V) +150°C -65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	==4 \A/
5-Pin SOT23	571mW
Derates above +70°C 5-Pin SOT23	7.10 mW/°C

II. Manufacturing Information

A. Description/Function: Micropower Single Supply Comparator + Precision Reference

B. Process: S12

C. Number of Device Transistors: 204

D. Fabrication Location: Oregon or California, USA

E. Assembly Location: Malaysia or Thailand

F. Date of Initial Production: January, 2000

III. Packaging Information

A. Package Type: 5-Lead SOT23

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-1501-0179

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 35 x 57 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Si

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 159 \times 2}$$
 (Chi square value for MTTF upper limit)
$$\lambda = 6.83 \times 10^{-9}$$
 Temperature Acceleration factor assuming an activation energy of 0.8eV
$$\lambda = 6.83 \times 10^{-9}$$

$$\lambda = 6.83 \text{ F.I.T.}$$
 (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5374) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1L).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The CM57Z-2 die type has been found to have all pins able to withstand a transient pulse of ± 1000 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA and/or ± 20 V.

Table 1Reliability Evaluation Test Results

MAX9040xEUK

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)			
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	159	0
Moisture Testi	ng (Note 2)			
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	355	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical St	ress (Note 2)			
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.

Note 2: Generic Process/Package data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

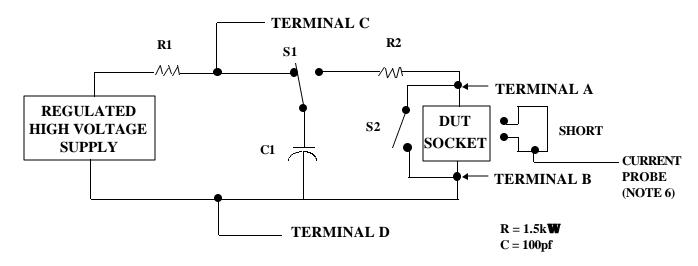
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

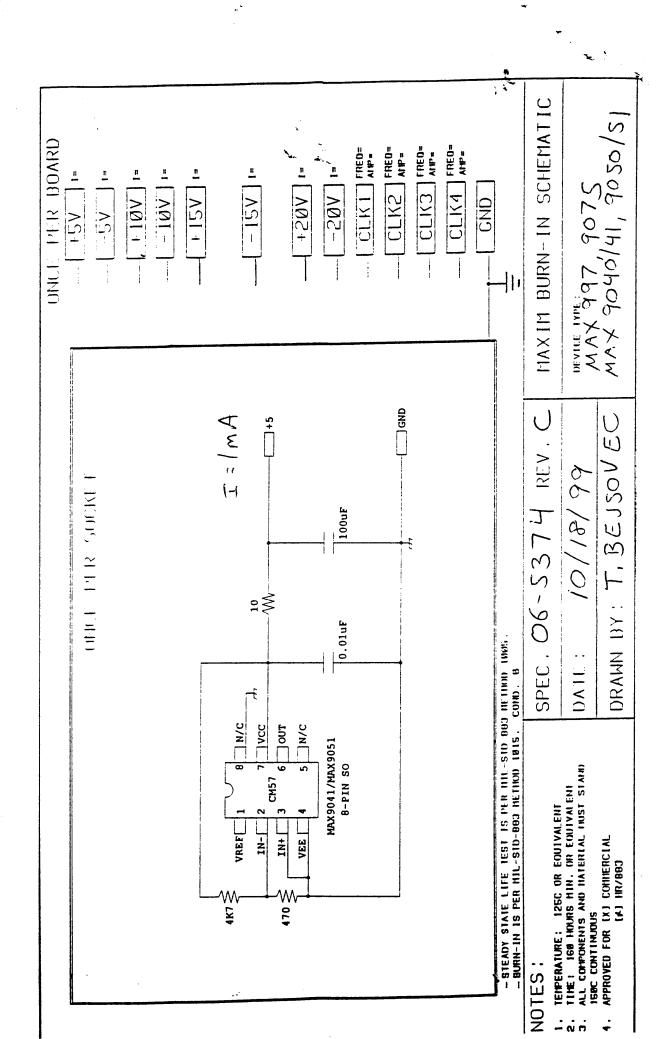
- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2}$ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

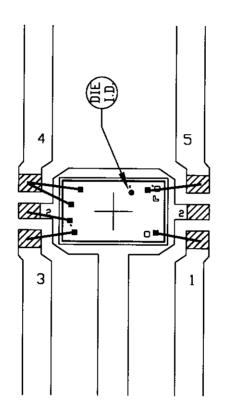
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \(\lambda_{S1} \), or \(\lambda_{S2} \) or \(\lambda_{S3} \) or \(\lambda_{CC1} \), or \(\lambda_{CC2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







Ø- B□NDING AREA

NOTE: CAVITY DOWN

PKG.CODE: U5-1		APPROVALS	DATE	/VI/IXI	111
CAV./PAD SIZE:	PKG.			BUILDSHEET NUMBER:	REV.:
64X45	DESIGN			05-1501-0179	Α