RELIABILITY REPORT

FOR

MAX8989EWL+T

WAFER LEVEL PRODUCTS

February 29, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX8989EWL+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8989 step-down converter is optimized for powering the power amplifier (PA) in multistandard handsets such as LTE, WCDMA, GSM, and EDGE. The device integrates a high-efficiency PWM step-down converter for medium- and low-power transmission with an 85mI (typ) low dropout (LDO) bypass regulator, in parallel with the step-down converter, enabling high-power transmission. The IC uses an analog input driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. The bypass LDO powers the PA directly from the battery during high-power transmission or in case of insufficient headroom between the input and programmed output. The bypass LDO is enabled when the output voltage is greater than 1.0V. In the case where the output current exceeds the step-down converter current limit, the bypass LDO provides supplementary current to the output, ensuring a stable output voltage. The bypass LDO also provides a smooth transition between step-down regulation and operation in dropout. The IC is available in a 9-bump, 1.6mm x 1.6mm WLP package (0.69mm max height).

II. Manufacturing Information

A. Description/Function:	Multi-mode PA Step-Down Converter with Linear Bypass Mode
B. Process:	S45
C. Number of Device Transistors:	6881
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Japan and USA
F. Date of Initial Production:	February 15, 2011

III. Packaging Information

A. Package Type:	9-bump WLP 3x3 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-4072
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	71°C/W
M. Multi Layer Theta Jc:	26°C/W

IV. Die Information

A. Dimensions:	63 X 63 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	2.7 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EJ2ZCQ001B, D/C 1021)

The PQ77 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX8989EWL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	EJ2ZCQ001B, D/C 1021

Note 1: Life Test Data may represent plastic DIP qualification lots.