

RELIABILITY REPORT
FOR
MAX894LESA
PLASTIC ENCAPSULATED DEVICES

February 17, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

A handwritten signature in black ink, appearing to read "J Pedicord".

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Reviewed by

A handwritten signature in black ink, appearing to read "Bryan J. Preeshl".

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX894L successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	
IV.Die InformationAttachments

I. Device Description

A. General

The MAX894L smart, dual, low-voltage, P-channel, MOSFET power switch is intended for high-side load-switching applications. This switch operates with inputs from +2.7V to +5.5V, making it ideal for both 3V and 5V systems. Internal current-limiting circuitry protects the input supply against overload. Thermal-overload protection limits power dissipation and junction temperature.

The MAX894L's maximum current limit is 500mA. The current limit through the switch is programmed with resistors from SET A/SET B to ground. When the switch is on, the quiescent supply current is a low 16 μ A. When the switch is off, the supply current decreases to 0.1 μ A.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN to GND	-0.3V to 6V
/ONA, /ONB to GND	-0.3V to 6V
SET A, SET B, OUT A, OUT B to GND	-0.3V to ($V_{IN} + 0.3V$)
Maximum Continuous Switch Current	0.75A
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
8-Pin NSO	471mW
Derates above +70°C	
8-Pin NSO	5.88W/°C

II. Manufacturing Information

A. Description/Function:	Dual, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown
B. Process:	S12 - Standard 1.2 micron silicon gate CMOS
C. Number of Device Transistors:	453
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	October, 1996

III. Packaging Information

A. Package Type:	8-Lead Small Outline
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1701-0354
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A:	Level 1

IV. Die Information

A. Dimensions:	68 x 132 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 320 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 3.39 \times 10^{-9} \quad \lambda = 3.39 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5187) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PW78-3 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX894LESA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		320	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

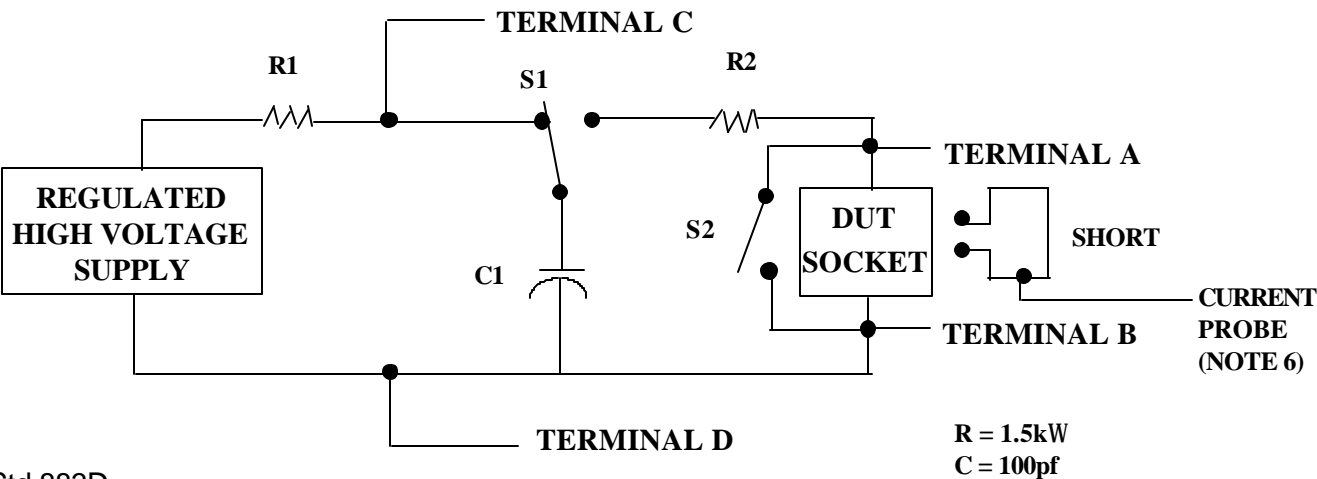
TABLE II. Pin combination to be tested. 1/ 2/

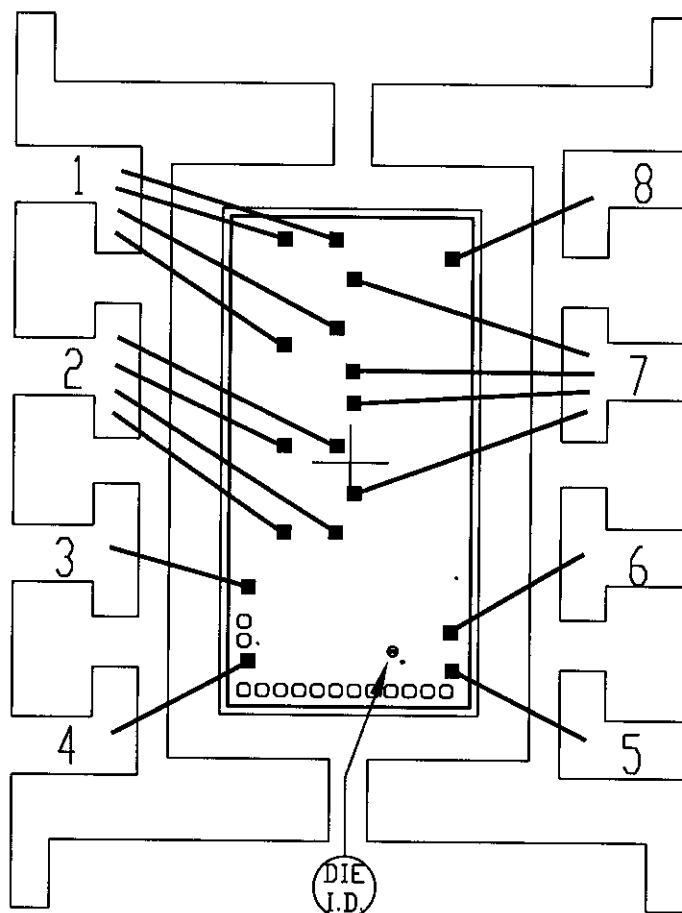
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

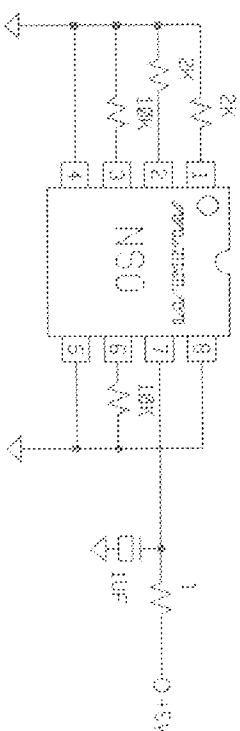




PKG.CODE: S8-5		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 95 X 155	PKG. DESIGN			BUILDSHEET NUMBER: 05-1701-0354	REV: A

ONCE PER BOARD

ONCE PER DEVICE



+5V I < 3mA

PS2 I =

PS3 I =

PS4 I =

PS5 I =

PS6 I =

CLK0 FREQ= ATP=

CLK1 FREQ= ATP=

CLK2 FREQ= ATP=

CLK3 FREQ= ATP=

CLK4 FREQ= ATP=

GND

STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 168 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 1500C CONTINUOUS
4. APPROVED FOR EX. COMMERCIAL
DO BE/263

SPEC. NO. 06-5187 REV: B

DATE: 8/26/96

DEVICE TYPE (S):

MAX8934/5/6

MAXIM BURN-IN SCHEMATIC IC