RELIABILITY REPORT

FOR

MAX8902BATA+

PLASTIC ENCAPSULATED DEVICES

Jun 3, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX8902BATA+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX8902A/MAX8902B low-noise linear regulators deliver up to 500mA of output current with only 16µVRMS of output noise in a 100kHz bandwidth. These regulators maintain their output voltage over a wide input range, requiring only 100mV of input-to-output headroom at full load. These LDOs maintain a low 80µA typical supply current, independent of the load current and dropout voltage. The regulator control circuitry includes a programmable soft-start circuit and short circuit, reverse current, and thermal-overload protection. Other features include an enable input and a power-OK output (MAX8902B only). The MAX8902A output voltage can be set to 1.5V, 1.8V, 2.0V, 2.5V, 3.0V, 3.1V, 3.3V, 4.6V, or 4.7V using the SELA and SELB inputs. The MAX8902B output voltage can be set between 0.6V and 5.3V with an external resistor voltage-divider.

II. Manufacturing Information

A. Description/Function:	Low-Noise 500mA LDO Regulators in a 2mm x 2mm TDFN Package
B. Process:	S4
C. Number of Device Transistors:	2937
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	NSEB
F. Date of Initial Production:	October 27, 2007

III. Packaging Information

A. Package Type:	8-pin TDFN 2x2
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2909
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Jc:	10.8°C/W
K. Multi Layer Theta Ja:	83.9°C/W
L. Multi Layer Theta Jc:	36.6°C/W

IV. Die Information

A. Dimensions:	31 X 57 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/Cu (Cu = 0.5%) w/ Ti/TiN barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

λ = 22.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S4 Process results in a FIT Rate of 0.28 @ 25C and 4.85 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PQ23-1 die type has been found to have all pins able to withstand a transient pulse of:

HBM ESD: +/-1500 V per JEDEC JESD22-A114
CDM ESD: +/-750 V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX8902BATA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data