

RELIABILITY REPORT FOR MAX8719ETA+T

PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineering



Conclusion

The MAX8719ETA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX8718/MAX8719 are micropower, 8-pin TDFN linear regulators that supply always-on, keep-alive power to CMOS RAM, real-time clocks (RTC), and microcontrollers in systems with high-voltage batteries. The circuits consist of a 100mA linear regulator and a power-good comparator (PGOOD) with fixed-output delay. Key features include wide input voltage range, low-dropout voltage, and low-quiescent supply current. Despite a miserly 25µA (max) no-load quiescent current, the MAX8718/MAX8719 have good line- and loadtransient response and excellent AC power-supply rejection. They provide a clean fixed 5V or 3.3V output (MAX8718), or an adjustable 1.24V to 28V output (MAX8719), even when subjected to fast supply-voltage changes that occur during the switchover from battery to AC-adapter input power. The space-saving TDFN package has excellent thermal characteristics and tolerates up to 1951mW of power dissipation. Internal foldback current limiting and thermal shutdown protect the regulator from overload and thermal faults. In addition to the main notebook-computer application, these devices are useful in other low-power, high-voltage applications (4V IN < 28V) such as smart batteries, current control loops, telecom emergency power, and housekeeping power for off-line supplies. The MAX8718/MAX8719 are available in a thermally enhanced 3mm x 3mm, 8-lead TDFN package.



II. Manufacturing Information

- A. Description/Function:High-Voltage, Low-Power Linear Regulators for Notebook ComputersB. Process:B12C. Fabrication Location:USA
 - D. Assembly Location:Taiwan, China, ThailandE. Date of Initial Production:October 23, 2004

III. Packaging Information

A. Package Type:	8-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1112
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8°C/W

IV. Die Information

A. Dimensions:	60 X 81 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet.0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$
 (Chi square value for MTTF upper limit)
(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)
$$\lambda = 23.4 \times 10^{-9}$$

x = 23.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B12 Process results in a FIT Rate of 0.06 @ 25°C and 1.06 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SRZ1BQ001B, D/C 0434)

The PD58-1 die type has been found to have all pins able to withstand an HBM transient pulse of +/-400V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.



Table 1 Reliability Evaluation Test Results

MAX8719ETA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (N	Note 1)				
	Ta = 135°C	DC Parameters	47	0	
	Biased	& functionality			
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.