RELIABILITY REPORT

FOR

MAX8566ETJ

PLASTIC ENCAPSULATED DEVICES

April 4, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX8566 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8566 high-efficiency switching regulator delivers up to 10A load current at output voltages from 0.6V to (0.87 x V_{IN}). The IC operates from 2.3V to 3.6V input supplies, making it ideal for point-of-load applications. The total output-voltage set error is less than ±1% over load, line, and temperature.

The MAX8566 operates in pulse-width-modulation (PWM) mode with a 250kHz to 2.4MHz switching frequency range that is programmable by an external resistor. The IC can be synchronized to an external clock in the same frequency range using the SYNC input. The high operating frequency minimizes the size of external components. Using low-$R_{DS(ON)}$ n-channel MOSFETs for both high- and low-side switches maintains high efficiency at both heavy-load and high-switching frequencies.

The MAX8566 employs a voltage-mode control architecture with a high-bandwidth (> 10MHz) error amplifier. The voltage-mode control architecture makes switching frequencies greater than 1MHz possible, achieving all-ceramic-capacitor designs to minimize PC board space. The error amplifier works with Type 3 compensation to fully utilize the bandwidth of the high-frequency switching to obtain fast transient response. Adjustable soft-start time provides flexibility to minimize input startup inrush current. An open-drain, power-good (PWRGD) signal goes high when the output reaches 90% of its regulation point.

The MAX8566 provides a SYNCOUT output to synchronize a second MAX8566 or a second regulator switching 180° out-of-phase with the first to reduce the input ripple current, which consequently reduces the input-capacitance requirements. The MAX8566 also provides an external reference input (REFIN) for output-tracking applications.

The MAX8566 is available in a 32-pin, 5mm x 5mm thin QFN package. The MAX8566 and all the required external components fit into a footprint of less than 0.80in^2.

B. Absolute Maximum Ratings

Item	Rating
EN/SS, EN, IN, SYNC, SKIP, VDD, LSS, PWRGD to GND	-0.3V to +4V (4.5V nonswitching)
SYNCOUT, SS, COMP, FB, REFIN, FREQ to GND	-0.3V to (VDD + 0.3V)
LX Current (Note 1)	-12A to +12A
BST to LX	-0.3V to +4V (4.5V nonswitching)
PGND to GND	-0.3V to +0.3V
Continuous Power Dissipation (TA = +85°C)	
32-Pin Thin QFN (derate 33.3mW/°C above +70°C)	2666.7W
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	High-Efficiency, 10A, PWM Internal-Switch Step-Down Regulator
B. Process:	S4
C. Number of Device Transistors:	7594
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	April, 2005

III. Packaging Information

A. Package Type:	**32-Pin TQFN (5x5)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (2.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-1156
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	85 x 115 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1, Metal2 & Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1, Metal2 & Metal3 = 0.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{100 \times 4340 \times 77 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 2.74 \times 10^{-9}$

λ = 2.74 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6358) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S4 Process results in a FIT Rate of 0.56 @ 25C and 9.60 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PN26-2 die type has been found to have all pins able to withstand a transient pulse of <±200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8566ETJ

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality		77	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TQFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

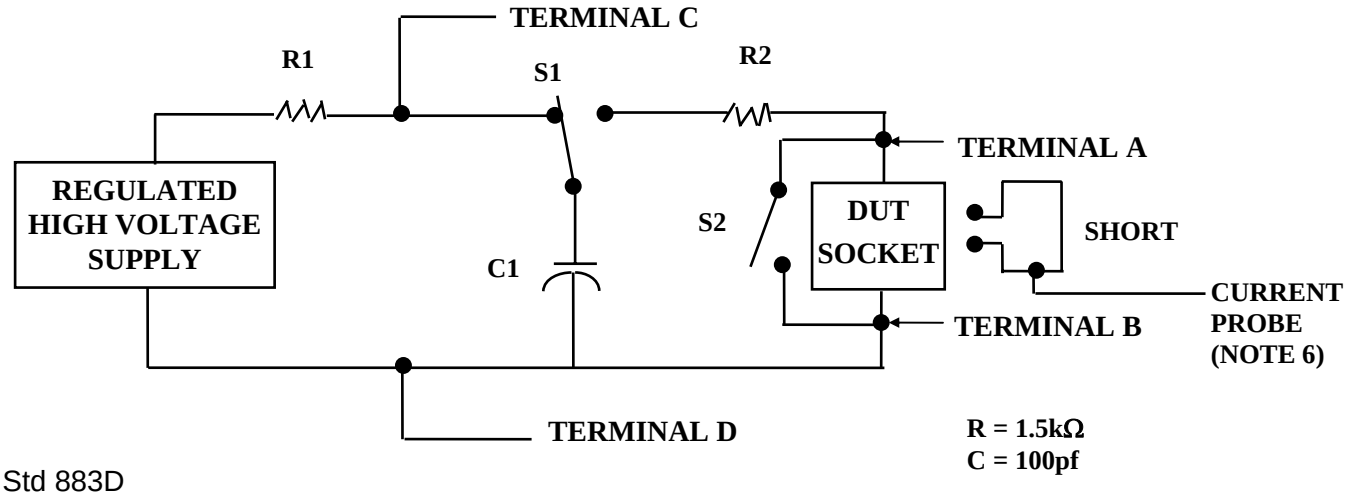
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

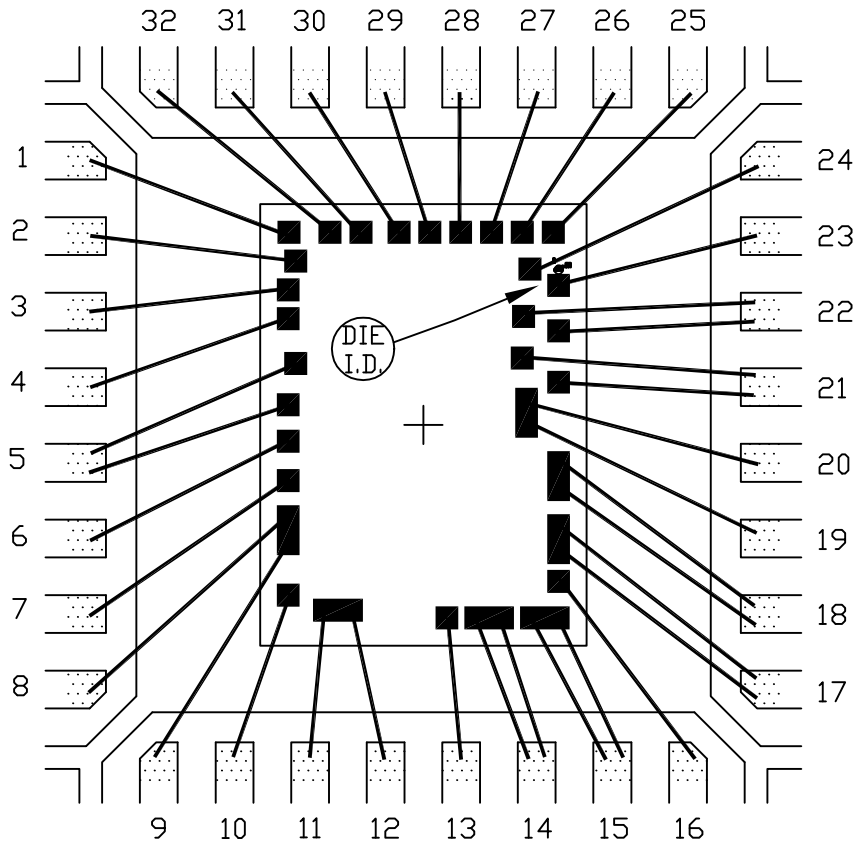
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



5x5x0.8mm THIN QFN PKG. EXPOSED PAD PKG.



*PINS5-12 HAVE SAME POTENTIAL (CONNECTED).
*PINS13-17 HAVE SAME POTENTIAL (CONNECTED).
*PINS18-22 HAVE SAME POTENTIAL (CONNECTED).

BONDABLE AREA

PKG. CODE: T3255-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 150x150	PKG.	Scott Schroeder	3/12/04	BOND DIAGRAM #: 05-9000-1156	REV: B
	DESIGN	Cory Arnold	3/16/04		

MAXIM ENGINEERING CHANGE NOTICE

ECN #	PAGE
HQ-04-B559	1 OF 3

TITLE: BI Circuit: MAX8566 (PN26Z)

DOC ID # 06-6358	NEW REV: C	OLD REV: B	EFFECTIVE: 02/02/05

TYPE	883 ☐	SMD ☐ #	PERMANENT ☒	TEMPORARY ☐ EXPIRES:

ORIGINATOR	Jim Cittadino	EXT: 4410	VP NAME: Doluca

OTHER DOC AFFECTED: NO ☒ YES ☐ LIST: ➔	
MATL. AFFECTED: NO ☒ YES ☐ ➔	USE AS IS: ☐ REWORK: ☐ SCRAP: ☐

***For Maxfab Lot Traveler Changes ONLY*: Affects version number?** NO ☐ YES ☐ **IF YES**, **ECN the Process Revision List.**

***For Data Sheet Changes ONLY*: Review Data Sheet before printing?** NO ☐ YES ☐ **IF YES**, **initial_____**

DESIGN CHANGES ONLY:

ROOT CAUSE:

CORRECTIVE ACTION:

REASON FOR CHANGE: Resistor value changed.

FROM:	TO:
4.7K	**6.8K**

DISTRIBUTION: ☒ **HQ** ☐ **Maxim North** ☐ **Maxfab South** **Manufacturing Areas:** _____
Offshore PH, _____ **Other** _____

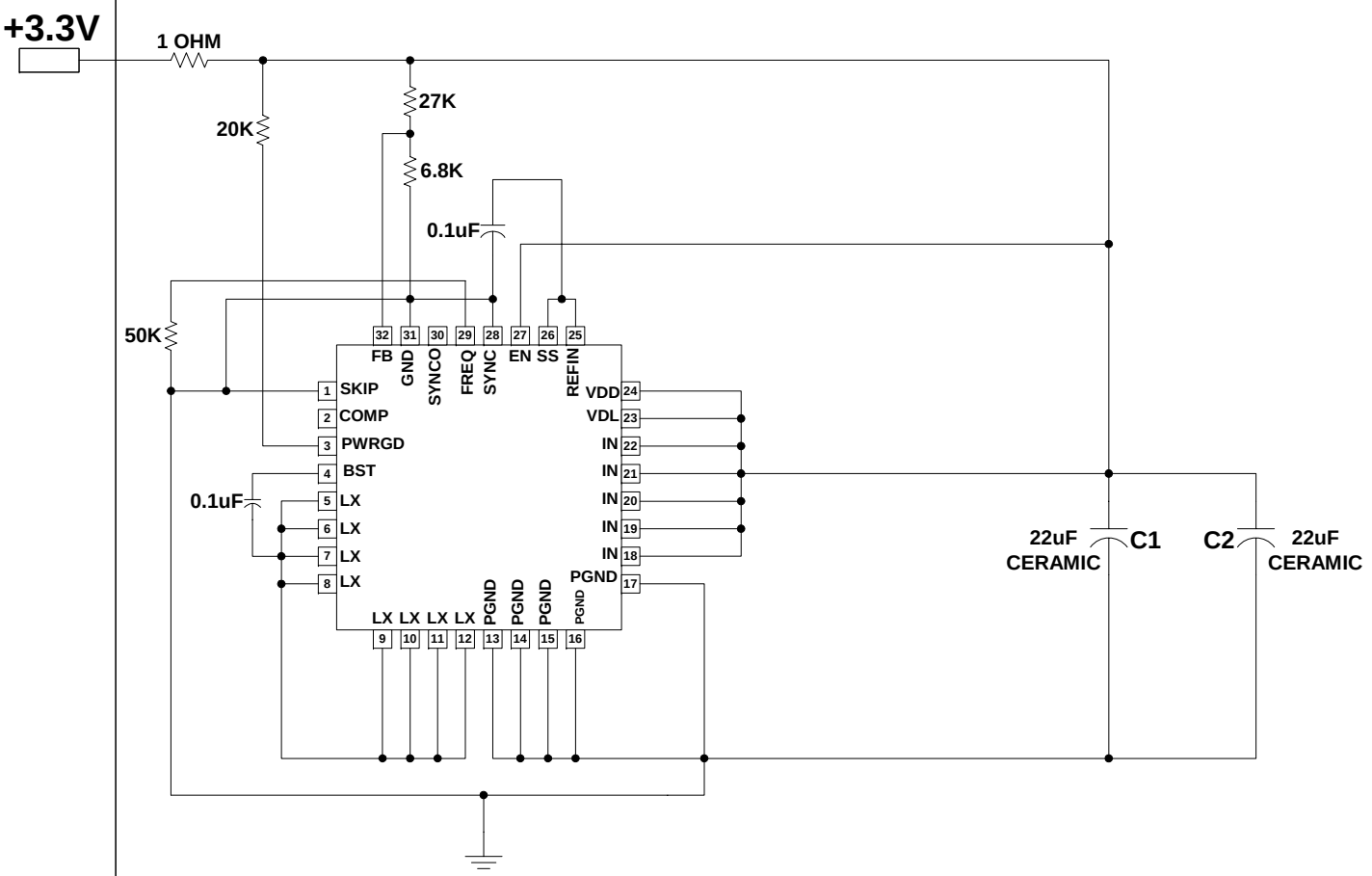
ORIGINAL APPROVALS ARE ON FILE IN THE N/A DOCUMENT CONTROL OFFICE.

APPROVALS	DATE	APPROVALS	DATE	APPROVALS	DATE
Jim Cittadino	12/20/04				
Cory Arnold	01/03/05				
Steve Skala	02/02/05				

Date ECN submitted into D.C.: 12/29/04 SA | **Document Control processor initials**: SA

ONCE PER BOARD

ONCE PER SOCKET



DEVICES: MAX8566 (PN26)
PACKAGE: 32-QFN 5x5 THIN
MAX EXPECTED CURRENT: 42mA

DRAWN BY: JIM CITTADINO
NOTES: PLACE C1 AND C2 AS CLOSE TO THE IC SOCKET AS POSSIBLE.

REVISION HISTORY

REV	CHANGES MADE	DATE	INIT.
A	ECN HQ-04-0466. Initial release.	3/5/04	JC
B	ECN HQ-04-4931. Package changed.	06/24/04	JC
C	ECN HQ-04-B559 Schematic revised.	02/02/05	JC

18-1058