MAX8539EEI
Rev. A

RELIABILITY REPORT

FOR

MAX8539EEI

PLASTIC ENCAPSULATED DEVICES

March 31, 2004

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX8539 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX8539 controller provides a complete power-management solution for both double-data-rate (DDR) and combiner supplies. The MAX8539 is configured for out-of-phase and in-phase DDR power-supply operations, respectively, and generates three outputs: the main memory voltage (V_{DDQ}), the tracking sinking/sourcing termination voltage (V_{TT}), and the termination reference voltage (V_{TTR}).

The MAX8539 uses constant-frequency voltage-mode architecture with operating frequencies of 200kHz to 1.4MHz. An internal high- bandwidth (25MHz) operational amplifier is used as an error amplifier to regulate the output voltage. This allows fast transient response, reducing the number of output capacitors. An all-N-FET design optimizes efficiency and cost. The MAX8539 has a 1% accurate reference. The second synchronous buck controller in the MAX8539 and the V_{TTR} amplifier generates 1/2 V_{DDQ} voltage for V_{TT} and V_{TTR}, and track the V_{DDQ} within ±1%.

The controller uses a high-side current-sense architecture for current limiting. ILIM pins allow the setting of an adjustable, lossless current limit for different combinations of load current and R_{DSON}. Alternately, more accurate overcurrent limit is achieved by using a sense resistor in series with the high-side FET. Overvoltage protection is achieved by latching off the high-side MOSFET and latching on the low-side MOSFET when the output voltage exceeds 17% of its set output. Independent enable, power-good, and soft-start features enhance flexibility.

B. Absolute Maximum Ratings

Item	Rating
V+ to GND	-0.3V to +25V
AVL, VL to GND	-0.3V to +6V
PGND to GND	-0.3V to +0.3V
FB_, EN_, POK_ to GND	-0.3V to +6V
REFIN, VTTR, FREQ, SS_, COMP_ to GND	.-0.3V to (AVL + 0.3V)
BST_, ILIM_ to GND	-0.3V to +30V
DH1 to LX1	-0.3V to (BST1 + 0.3V)
DH2 to LX2	-0.3V to (BST2 + 0.3V)
LX_ to BST_	-6V to +0.3V
LX_ to GND	-2V to +25V
DL_ to PGND	-0.3V to (VL + 0.3V)
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin QSOP	860mW
Derates above +70°C	
28-Pin QSOP	10.8mW/°C

II. Manufacturing Information

A. Description/Function: Dual-Synchronous Buck Controllers for Point-of-Load, Tracking, and DDR Memory Power Supplies

B. Process: S8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 5504

D. Fabrication Location: California, USA

E. Assembly Location: Philippines or Thailand

F. Date of Initial Production: January, 2004

III. Packaging Information

A. Package Type: **28-Pin QSOP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-Filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-9000-0559

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A: Level 1

IV. Die Information

A. Dimensions: 140 x 80 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)

F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

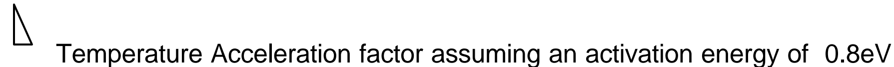
D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)



Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$

$\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6190) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PN02-2 die type has been found to have all pins able to withstand a transient pulse of ±<200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8539EEI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

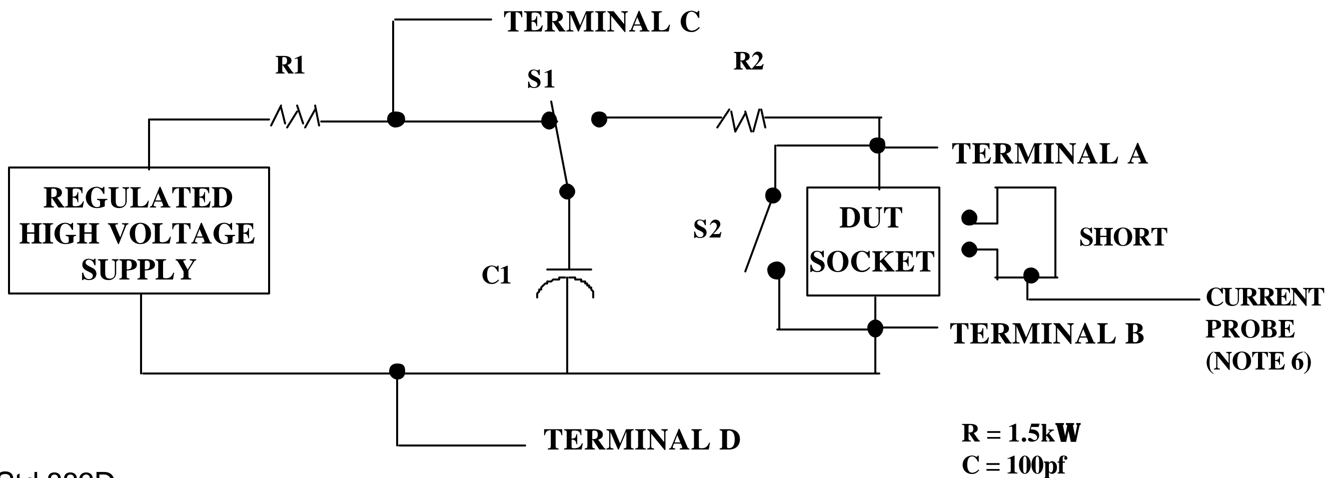
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

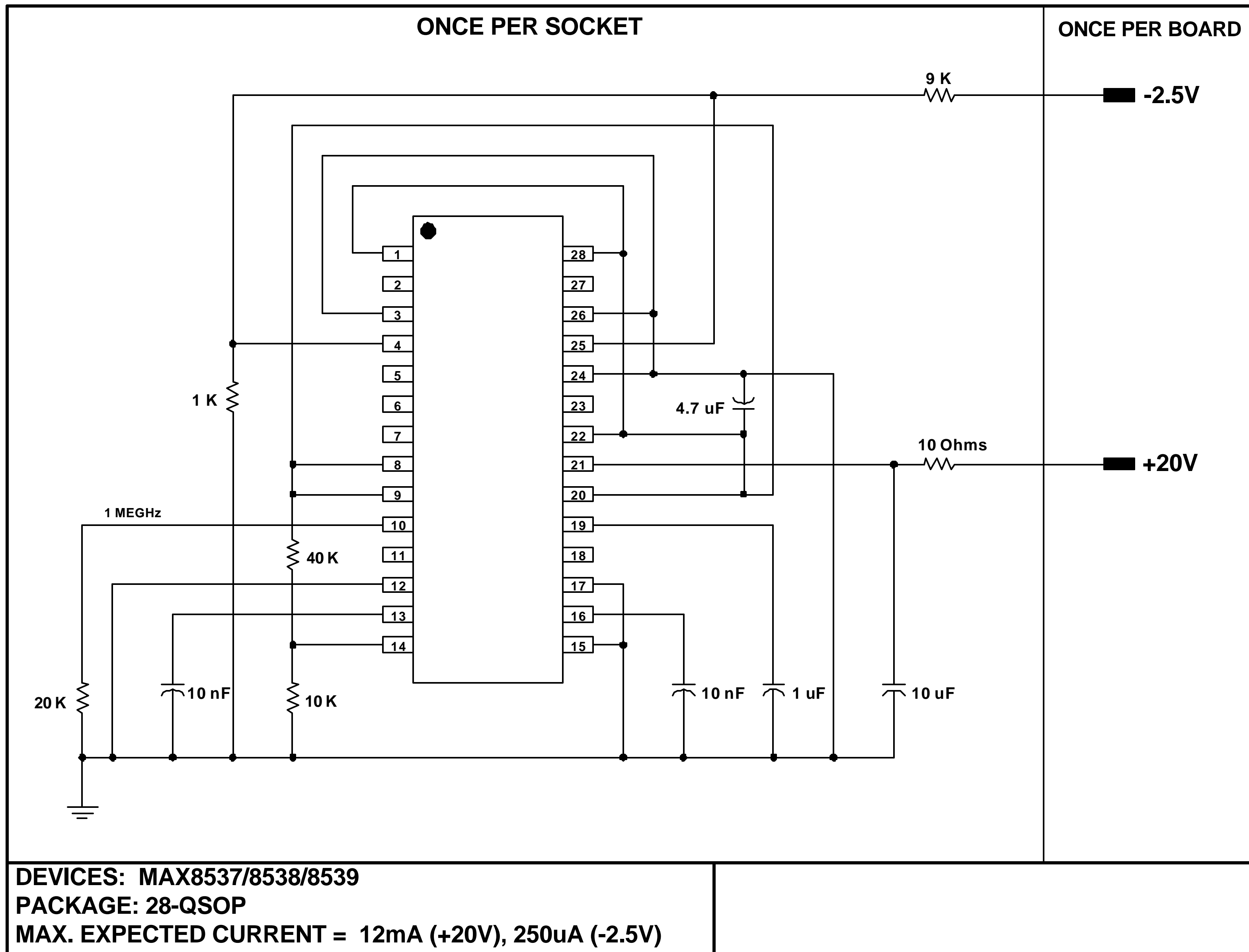


1 2 3 4 5 6 7 8 9 10 11 12 13 14

28 27 26 25 24 23 22 21 20 19 18 17 16 15

0.015

DIE I.D.


ONCE PER SOCKET
ONCE PER BOARD
9 K
-2.5V
10 Ohms
+20V
1 K
4.7 uF
1 MEGHz
40 K
20 K
10 nF
10 K
10 nF
1 uF
10 uF
1
2
3
4
5
6
7
8
9
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11
12
13
14
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28
DEVICES: MAX8537/8538/8539
PACKAGE: 28-QSOP
MAX. EXPECTED CURRENT = 12mA (+20V), 250uA (-2.5V)