MAX8517EUB
Rev. A

RELIABILITY REPORT

FOR

MAX8517EUB

PLASTIC ENCAPSULATED DEVICES

August 15, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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Conclusion

The **MAX8517** has completed qualification testing except for product level Burn-In. Package and Process qualification has been completed for the device.

Table of Contents

I. Device Description

A. General

The MAX8517 low-dropout linear regulator operateS from input voltages as low as 1.425V and is able to deliver up to 1A of continuous output current with a maximum dropout voltage of only 200mV. The output voltage can be set from 0.5V to (V_{IN} - 0.2V) and is 1.4% accurate over load and line variations, from 0°C to +85°C.

These regulator uses small, 1µF ceramic input capacitors and 4.7µF ceramic output capacitors to deliver 1A output current. High bandwidth provides excellent transient response and limits the output voltage deviation to 45mV for a 20mA to 1A load step, with only a 4.7µF ceramic output capacitor, and the voltage deviations can be reduced further by increasing the output capacitor.

Designed with an internal p-channel MOSFET pass transistor, the MAX8517 features low 340µA (typ) supply current during dropout conditions. Soft-start reduces inrush current. Other features include a logic-controlled shutdown mode, short-circuit protection, and thermal-overload protection.

The MAX8517 features a power-OK (POK) output that transitions high when the regulator output is within ±10% of its nominal output voltage.

The part is packaged in a 10-pin µMAX® package that includes an exposed pad for optimal power dispation.

B. Absolute Maximum Ratings

Item	Rating
IN, EN, POK (MAX8517), POR (MAX8518), FB to GND	-0.3V to +4.0V
OUT to GND	-0.3V to (IN + 0.3V)
Output Short-Circuit Duration	Continuous
Continuous Power Dissipation (TA = +70°C, EP soldered to PC board ground)	
10-Pin µMAX (derate 10.3mW/°C above +70°C)	824mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	1.425V to 3.6V Input, 1A, 0.2V Dropout LDO Regulators
B. Process:	S4
C. Number of Device Transistors:	2849
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or Philippines
F. Date of Initial Production:	April, 2004

III. Packaging Information

A. Package Type:	**10-Pin uMAX**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0163
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	60 x 65 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1, Metal2 & Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1, Metal2 & Metal3 = 0.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 95 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 11.57 \times 10^{-9}$

λ = 11.57 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6118) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S4 Process results in a FIT Rate of 0.37 @ 25C and 6.28 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PM63Y die type has been found to have all pins able to withstand a transient pulse of ±2500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8517EUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		95	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	10-Pin uMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

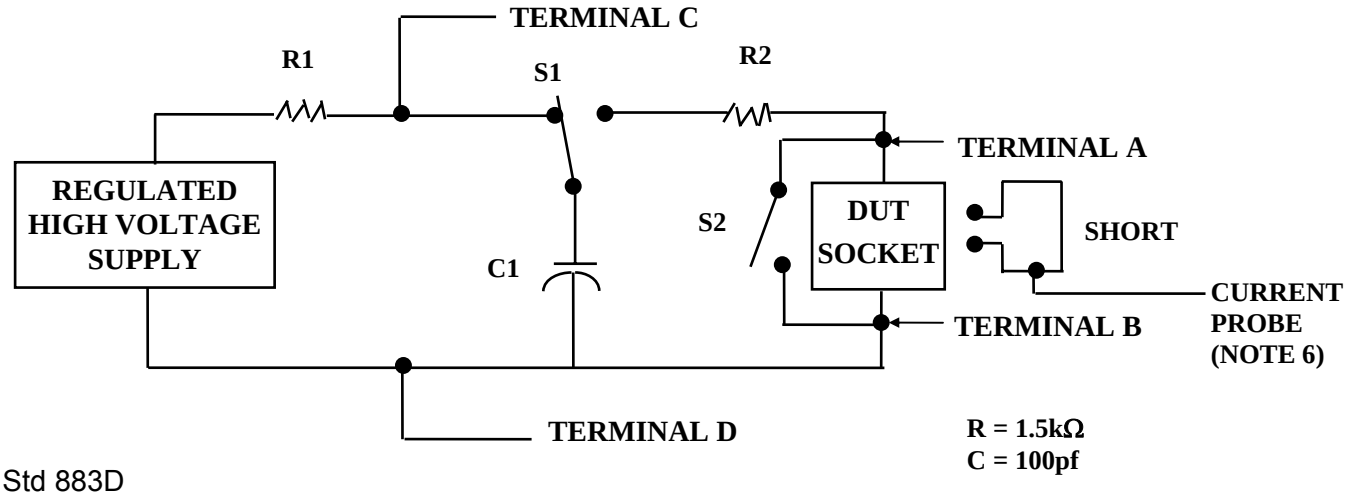
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

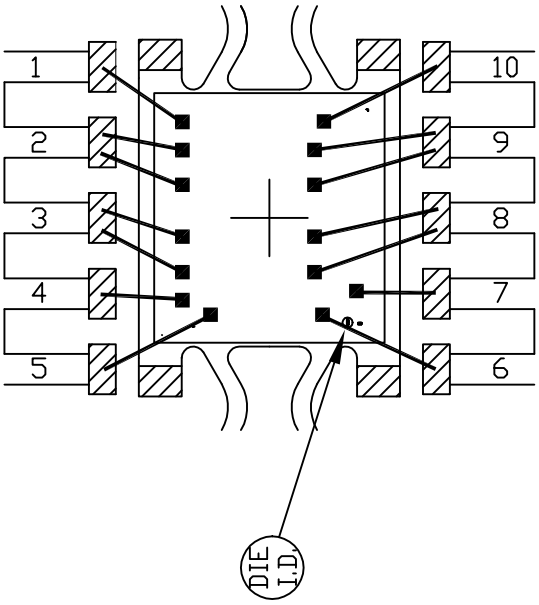
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



EXPOSED PAD PKG.

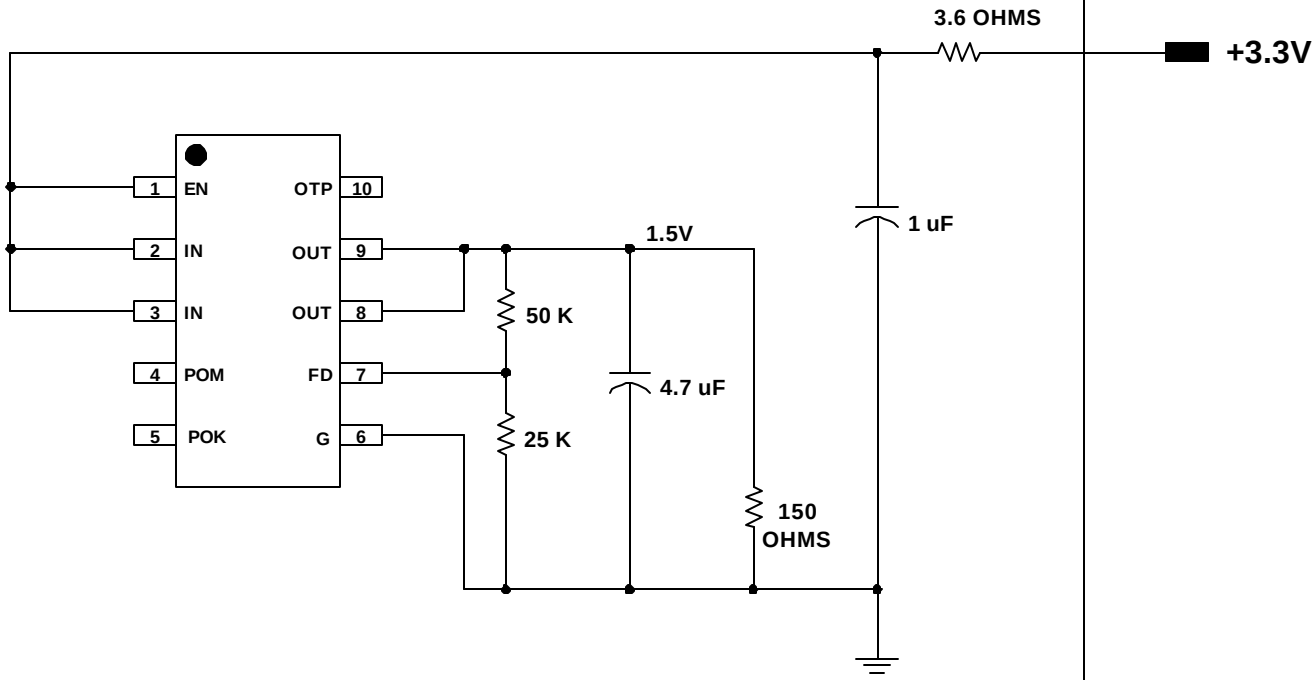


BONDABLE AREA

PKG. CODE: U10E-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x73	PKG.			BOND DIAGRAM #: 05-9000-0163	REV: B
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 8516/7/8
PACKAGE: 10-uMAX
MAX. EXPECTED CURRENT = 11mA