RELIABILITY REPORT

FOR

MAX8512ETA+

PLASTIC ENCAPSULATED DEVICES

December 1, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX8512ETA+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8510/MAX8511/MAX8512 ultra-low-noise, low-dropout (LDO) linear regulators are designed to deliver up to 120mA continuous output current. These regulators achieve a low 120mV dropout for 120mA load current. The MAX8510 uses an advanced architecture to achieve ultra-low output voltage noise of 11µVRMS and PSRR of 54dB at 100kHz. The MAX8511 does not require a bypass capacitor, hence achieving the smallest PC board area. The MAX8512's output voltage can be adjusted with an external divider. The MAX8510/MAX8511 are preset to a variety of voltages in the 1.5V to 4.5V range. Designed with a P-channel MOSFET series pass transistor, the MAX8510/MAX8511/MAX8512 maintain very low ground current (40µA). The regulators are designed and optimized to work with low-value, low-cost ceramic capacitors. The MAX8510 requires only 1µF (typ) of output capacitance for stability with any load. When disabled, current consumption drops to below 1µA. Package options include a 5-pin SC70 and a tiny 2mm x 2mm x 0.8mm TDFN package.

II. Manufacturing Information

A. Description/Function:	Ultra-Low-Noise, High PSRR, Low-Dropout, 120mA Linear Regulators
B. Process:	B8
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	UTL Thailand
F. Date of Initial Production:	January 25, 2003

III. Packaging Information

A. Package Type:	8-pin TDFN 2x2
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2522
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	10.8°C/W
L. Multi Layer Theta Ja:	83.9°C/W
M. Multi Layer Theta Jc:	36.6°C/W

IV. Die Information

A. Dimensions:	31 X 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.8 \times 10^{-9}$

$\lambda = 22.8$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the B8 Process results in a FIT Rate of 2.71 @ 25C and 17.30 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PM21-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX8512ETA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data