MAX7318AxG
Rev. A

RELIABILITY REPORT

FOR

MAX7318AxG

PLASTIC ENCAPSULATED DEVICES

July 13, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Conclusion

The MAX7318 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX7318 2-wire-interfaced expander provides 16-bit parallel input/output (I/O) port expansion for SMBus™ and I2C* applications. The MAX7318 consists of input port registers, output port registers, polarity inversion registers, configuration registers, a bus timeout register, and an I2C-compatible serial interface logic compatible with SMBus. The system master can invert the MAX7318 input data by writing to the activehigh polarity inversion register.

Any of the 16 I/O ports can be configured as an input or output. A power-on reset (POR) initializes the 16 I/Os as inputs. Three address select pins configure one of 64 slave ID addresses.

The MAX7318 supports hot insertion. All port pins, the INT-bar output, SDA, SCL, and the slave address inputs AD0-2 remain high impedance in power-down (V+ = 0V) with up to 6V asserted upon them.

The MAX7318 is available in 24-pin SO, SSOP, TSSOP, and thin QFN packages and is specified over the -40°C to +125°C automotive temperature range.

For applications requiring an SMBus timeout function, refer to the MAX7311 data sheet.

B. Absolute Maximum Ratings

Item	Rating
V+ to GND	-0.3V to +6V
I/O0–I/O15 as Inputs	(GND - 0.3V) to +6V
SCL, SDA, AD0, AD1, AD2, INT	(GND - 0.3V) to +6V
Maximum V+ Current	+250mA
Maximum GND Current	-250mA
DC Input Current on I/O0–I/O15	±20mA
DC Output Current on I/O0–I/O15	±80mA
Continuous Power Dissipation (TA = +70°C)	
24-Pin Wide SO (derate 11.8mW/°C above +70°C)	941mW
24-Pin SSOP (derate 8.0mW/°C above +70°C)	640mW
24-Pin TSSOP (derate 12.2mW/°C above +70°C)	976mW
24-Pin Thin QFN (derate 20.8mW/°C above +70°C)	1667mW
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function: 2-Wire-Interfaced, 16-Bit, I/O Port Expander with Interrupt and Hot-Insertion Protection

B. Process: B6

C. Number of Device Transistors: 12,994

D. Fabrication Location: California, USA

E. Assembly Location: Malaysia, Philippines or Thailand

F. Date of Initial Production: April, 2002

III. Packaging Information

A. Package Type:	24-pin Wide SO	24-pin SSOP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0115	# 05-9000-0116
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

A. Package Type:	24-pin Thin QFN	24-pin TSSOP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0413	# 05-9000-0114
I. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	85 x 91 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 93 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

λ = 11.82 x 10-9

λ = 11.82 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-6053) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1N). Current monitor data for the B6/S6 Process results in a FIT rate of 0.28 @ 25°C and 4.88 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The DW53-2 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX7318AxG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		93	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	Wide SO SSOP TSSOP Thin QFN	77 77 77 77	0 0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

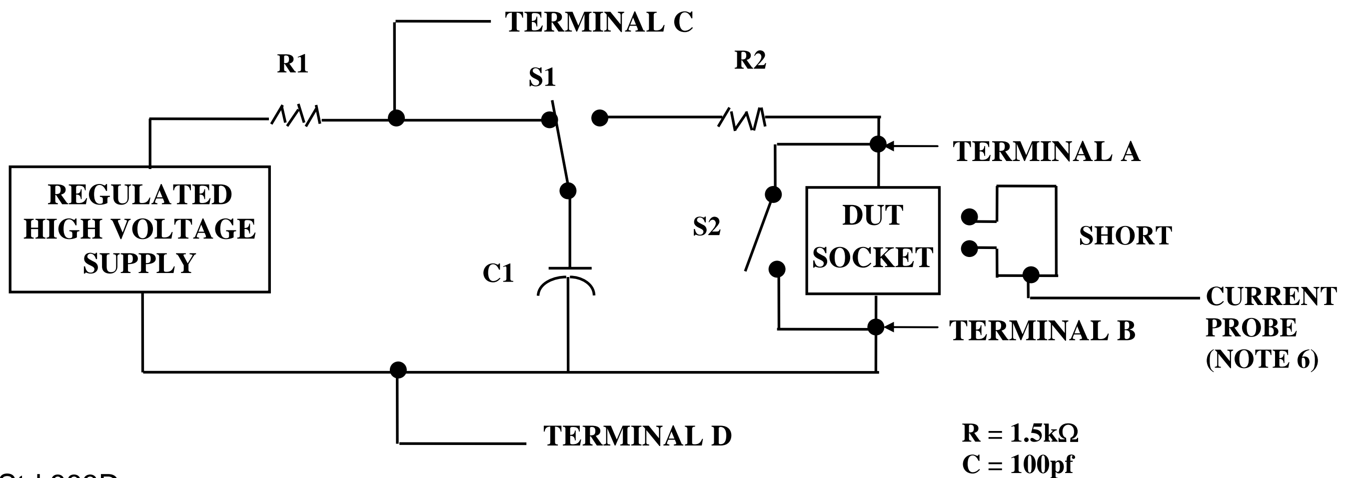
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



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DIE I.D.

PKG. CODE: A24-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 154X169	PKG.			BOND DIAGRAM #: 05-9000-0116	REV: A
	DESIGN				

3 2 1 24 23 22

4 21

5 20

6 19

7 18

8 17

9 16

10 11 12 13 14 15

DIE I.D.

1 2 3 4 5 6 7 8 9 10 11 12

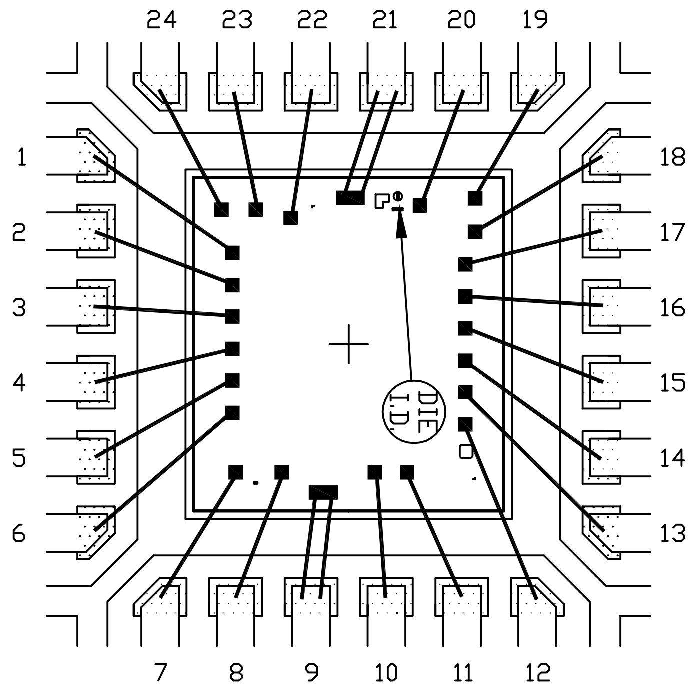
24 23 22 21 20 19 18 17 16 15 14 13

DIE I.D.

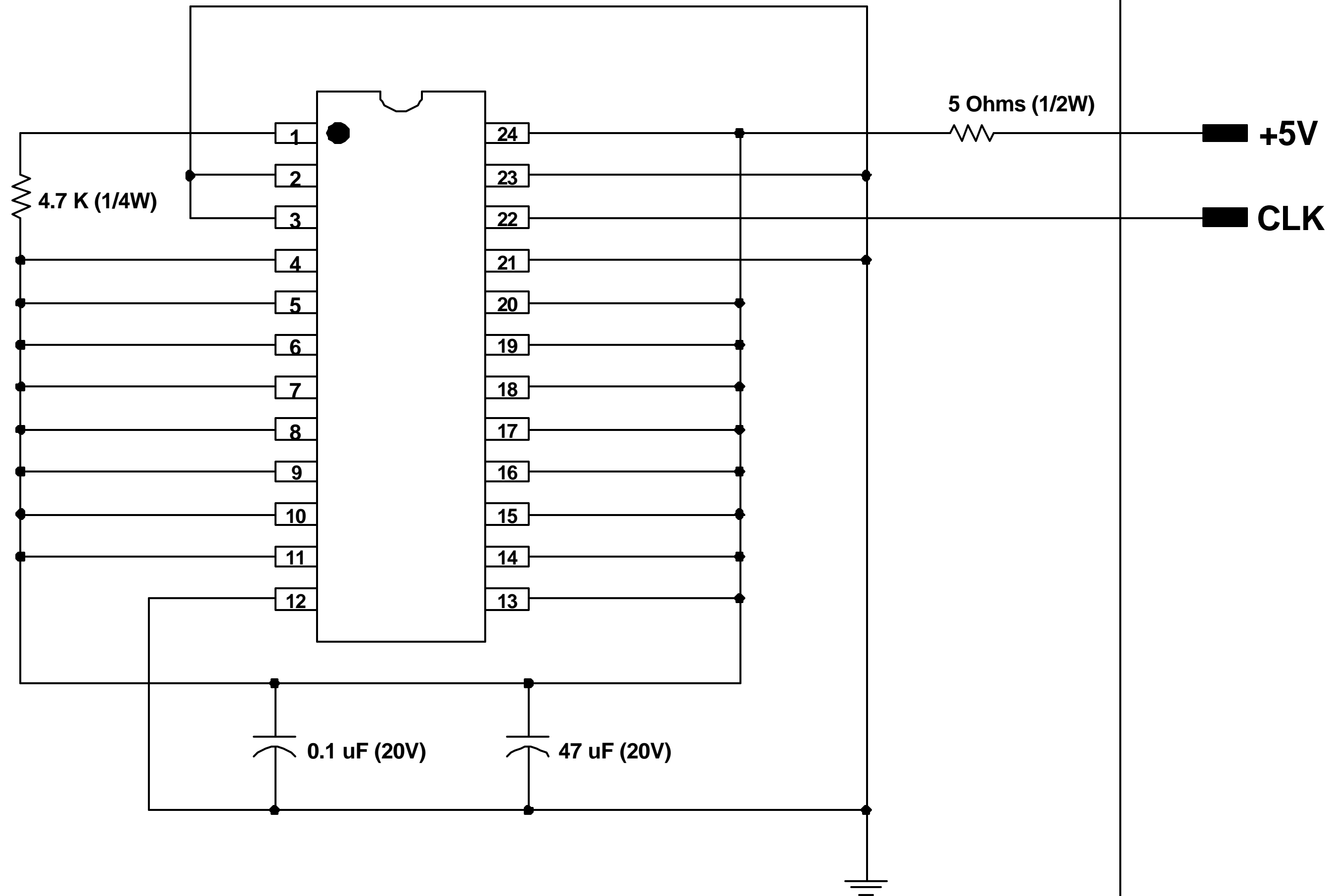
PKG. CODE: U24-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x217	PKG.			BOND DIAGRAM #: 05-9000-0114	REV: A
	DESIGN				

4x4x0.8mm THIN QFN PKG.

EXPOSED PAD PKG.



PKG. CODE: T2444-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE:	PKG.			BOND DIAGRAM #:	REV:
110x110	DESIGN			05-9000-0413	B



DEVICES: MAX 7311 DW53Z
PACKAGE: 24-SSOP
MAX. EXPECTED CURRENT = 15mA

NOTES: CLK = 200 KHz , 0V-5V, Free Running Clock.