

RELIABILITY REPORT FOR MAX7310EUE+ PLASTIC ENCAPSULATED DEVICES

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# MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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#### Conclusion

The MAX7310EUE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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#### I. Device Description

A. General

The MAX7310 provides 8-bit parallel input/output port expansion for SMBus<sup>™</sup>-compatible and I<sup>2</sup>C-compatible applications. The MAX7310 consists of an input port register, an output port register, a polarity inversion register, a configuration register, a bus timeout register, and an SMBus/I<sup>2</sup>C-compatible serial interface. The system master can invert the MAX7310 input data by writing to the active-high polarity inversion register. The system master can enable or disable bus timeout by writing to the bus timeout register.

Any of the eight I/O ports can be configured as input or output. An active-low reset input sets the eight I/Os as inputs. Three address-select pins configure one of 56 slave ID addresses.

The MAX7310 is available in 16-pin thin QFN, TSSOP, and QSOP packages and is specified over the -40°C to +125°C automotive temperature range.



- II. Manufacturing Information
  - A. Description/Function:
  - B. Process:
  - C. Number of Device Transistors:
  - D. Fabrication Location:
  - E. Assembly Location:
  - F. Date of Initial Production:

## III. Packaging Information

A. Package Type:	16-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0030
H. Flammability Rating:	Class UL94-V0
<ol> <li>Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C</li> </ol>	Level 1
J. Single Layer Theta Ja:	106°C/W
K. Single Layer Theta Jc:	27°C/W
L. Multi Layer Theta Ja:	90°C/W
M. Multi Layer Theta Jc:	27°C/W

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

C6

California

1/25/2003

Philippines, Thailand, Malaysia

#### IV. Die Information

A.	Dimensions:	70 X 78 mils
В.	Passivation:	$Si_3N_4\!/SiO_2$ (Silicon nitride/ Silicon dioxide)
C.	Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D.	Backside Metallization:	None
E.	Minimum Metal Width:	0.6 microns (as drawn)
F.	Minimum Metal Spacing:	0.6 microns (as drawn)
G.	Bondpad Dimensions:	5 mil. Sq.
н.	Isolation Dielectric:	SiO <sub>2</sub>
I.	Die Separation Method:	Wafer Saw



#### V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering)		
		Bryan Preeshl (Managing Director of QA)		
В.	Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet.		
		0.1% For all Visual Defects.		
C.	Observed Outgoing Defect Rate:	< 50 ppm		
D.	Sampling Plan:	Mil-Std-105D		

### VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (  $\lambda$ ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{\frac{1.83}{192 \times 4340 \times 45 \times 2}}_{(\text{where } 4340 = \text{Temperature Acceleration factor assuming an activation energy of 0.8eV})$  $\lambda = 23.9 \times 10^{-9}$  $\lambda = 23.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$ 

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the C6 Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

#### B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The DW52 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.



# Table 1 Reliability Evaluation Test Results

#### MAX7310EUE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES		
Static Life Test (Note 1)						
	Ta = 135°C	DC Parameters	45	0		
	Time = 192 hrs.	& functionality				
Moisture Testing (Note 2)						
HAST	Ta = 130°C	DC Parameters	77	0		
	RH = 85%	& functionality				
	Biased					
	Time = 96hrs.					
Mechanical Stress (Note 2)						
Temperature	-65°C/150°C	DC Parameters	77	0		
Cycle	1000 Cycles	& functionality				
	Method 1010					

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data