RELIABILITY REPORT

FOR

MAX7304AWA+T / MAX7304ATG+T

WAFER LEVEL PRODUCTS / PLASTIC ENCAPSULATED PRODUCTS

November 22, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX7304AWA+T / MAX7304ATG+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX7304 consists of 16 port GPIOs, with 12 pushpull GPIOs and four open-drain GPIOs configurable as PWM-controlled LED drivers. The device supports a 1.62V to 3.6V separate power supply for level translation. An address-select input (AD0) allows up to four unique slave addresses for the device.

Each GPIO can be programmed to one of the two externally applied logic voltage levels. PORT15–PORT12 can also be configured as LED drivers that feature constant-current sinks and PWM intensity control with the internal oscillator. The maximum constant-current level for each open-drain LED port is 20mA. The intensity of the LED on each open-drain port can be individually adjusted through a 256-step PWM control. The port also features LED fading. The same index rows and columns in the device can be used as a direct logic-level translator.

The device is offered in a 24-pin (3.5mm x 3.5mm) TQFN package with an exposed pad, and a small 25-bump (2.159mm x 2.159mm) wafer-level package (WLP) for cell phones, pocket PCs, and other portable consumer electronic applications. The device operates over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	I2C-Interfaced 16-Port, Level-Translating GPIO and LED Driver with High Level of Integrated ESD Protection	
B. Process:	S18	
C. Number of Device Transistors:	93400	
D. Fabrication Location:	USA	
E. Assembly Location:	Japan and USA	Taiwan and Thailand
F. Date of Initial Production:	June 23, 2011	

III. Packaging Information

A. Package Type:	25-bump WLP 5x5	24-pin TQFN 3.5x3.5
B. Lead Frame:	N/A	Copper
C. Lead Finish:	N/A	100% matte Tin
D. Die Attach:	N/A	Conductive
E. Bondwire:	N/A (N/A mil dia.)	Au (1 mil dia.)
F. Mold Material:	N/A	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4351	05-9000-4353
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	°C/W	65.1°C/W
K. Single Layer Theta Jc:	°C/W	5°C/W
L. Multi Layer Theta Ja:	52°C/W	65.1°C/W
M. Multi Layer Theta Jc:	°C/W	5.4°C/W

IV. Die Information

A. Dimensions:	85 X 85 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 2.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 2454 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 24.6 \times 10^{-9}$

$\lambda = 24.6$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.06 @ 25C and 1.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot VY0ZAQ001C, D/C 1114)

The DX49 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD gun (contact):	+/- 8kV PORT pins per IEC61000-4-2
ESD gun (air gap):	+/- 15kV PORT pins per IEC61000-4-2

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX7304AWA+T / MAX7304ATG+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 125C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	VY0ZAQ001D, D/C 1114

Note 1: Life Test Data may represent plastic DIP qualification lots.