RELIABILITY REPORT

FOR

MAX6965AEE+

PLASTIC ENCAPSULATED DEVICES

March 2, 2010

MAXIM INTEGRATED PRODUCTS

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Approved by
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Quality Assurance
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Conclusion

The MAX6965AEE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX6965 I²C-compatible serial interfaced peripheral provides microprocessors with nine additional output ports. Each output is an open-drain current-sinking output rated to 50mA at 7V. All outputs are capable of driving LEDs, or providing logic outputs with external resistive pullup up to 7V. Eight-bit PWM current control is also integrated. Four of the bits are global control and apply to all LED outputs to provide coarse adjustment of current from fully off to fully on with 14 intensity steps. Additionally each output then has an individual 4-bit control, which further divides the globally set current into 16 more steps. Alternatively, the current control can be configured as a single 8-bit control that sets all outputs at once. Each output has independent blink timing with two blink phases. LEDs can be individually set to be either on or off during either blink phase, or to ignore the blink control. The blink period is controlled by an external clock (up to 1kHz) on BLINK or by a register. The BLINK input can also be used as a logic control to turn the LEDs on and off, or as a general-purpose input (GPI). The MAX6965 supports hot insertion. The SDA, SCL, active-low RST, BLINK, and the slave address input AD0 remain high impedance in power-down (V+ = 0V) with up to 6V asserted upon them. The output ports remain high impedance with up to 8V asserted upon them. The MAX6965 is controlled through a 2-wire I²C serial interface, and can be configured to one of four I²C addresses.

II. Manufacturing Information

A. Description/Function:	9-Output LED Driver with Intensity Control and Hot-Insertion Protection
B. Process:	S4
C. Number of Device Transistors:	0
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	October 25, 2003

III. Packaging Information

A. Package Type:	16-pin QSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0793
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	120°C/W
K. Single Layer Theta Jc:	37°C/W
L. Multi Layer Theta Ja:	103.7°C/W
M. Multi Layer Theta Jc:	37°C/W

IV. Die Information

A. Dimensions:	60 X 58 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.05 @ 25C and 0.83 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The DW74-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA.

Table 1
Reliability Evaluation Test Results

MAX6965AEE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data