RELIABILITY REPORT

FOR

MAX6955APL+

PLASTIC ENCAPSULATED DEVICES

December 3, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX6955APL+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX6955 is a compact display driver that interfaces microprocessors to a mix of 7-segment, 14-segment, and 16-segment LED displays through an I²C-compatible 2-wire serial interface. The MAX6955 drives up to 16 digits 7-segment, 8 digits 14-segment, 8 digits 16-segment, or 128 discrete LEDs, while functioning from a supply voltage as low as 2.7V. The driver includes five I/O expander or general-purpose I/O (GPIO) lines, some or all of which can be configured as a key-switch reader. The key-switch reader automatically scans and debounces a matrix of up to 32 switches. Included on chip are full 14- and 16-segment ASCII 104-character fonts, a hexadecimal font for 7-segment displays, multiplex scan circuitry, anode and cathode drivers, and static RAM that stores each digit. The maximum segment current for the display digits is set using a single external resistor. Digit intensity can be independently adjusted using the 16-step internal digital brightness control. The MAX6955 includes a low-power shutdown mode, a scan-limit register that allows the user to display from 1 to 16 digits, segment blinking (synchronized across multiple drivers, if desired), and a test mode, which forces all LEDs on. The LED drivers are slew-rate limited to reduce EMI. For an SPI(tm)-compatible version, refer to the MAX6954 data sheet. An evaluation kit (EV kit) for the MAX6955 is available.

II. Manufacturing Information

A. Description/Function:	2-Wire Interfaced, 2.7V to 5.5V LED Display Driver with I/O Expander and Key Scan
B. Process:	TS50
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines
F. Date of Initial Production:	July 27, 2002

III. Packaging Information

A. Package Type:	40-pin PDIP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-3301-0030
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	60°C/W
K. Single Layer Theta Jc:	20°C/W

IV. Die Information

A. Dimensions:	132 X 147 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.50µm
F. Minimum Metal Spacing:	0.50µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.05}{192 \times 4340 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 52.7 \times 10^{-9}$

λ = 52.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS50 Process results in a FIT Rate of 0.25 @ 25C and 6.11 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The DW12 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-100 mA.

Table 1

Reliability Evaluation Test Results

MAX6955APL+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	1
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data