

RELIABILITY REPORT

FOR

MAX6951CEE+

PLASTIC ENCAPSULATED DEVICES

March 30, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by					
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Quality Assurance					
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Conclusion

The MAX6951CEE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX6950/MAX6951 are compact common-cathode display drivers that interface microprocessors to individual 7-segment numeric LED digits, bar graph, or discrete LEDs through an SPI(tm)-, QSPI(tm)-, MICROWIRE(tm)-compatible serial interface. The supply voltage can be as low as 2.7V. The MAX6950 drives up to five 7-segment digits or 40 discrete LEDs. The MAX6951 drives up to eight 7-segment digits or 64 discrete LEDs. Included on-chip are hexadecimal character decoders (0-9, A-F), multiplex scan circuitry, segment and digit drivers, and a static RAM that stores each digit. The user may select hexadecimal decoding or no-decode for each digit to allow any mix of 7-segment digits, bar graph, or discrete LEDs to be driven. The segment current for the LEDs is set by an internal digital brightness control. The segment drivers are slew-rate limited to reduce EMI. Individual digits may be addressed and updated without rewriting the entire display. The devices include a low-power shutdown mode, digital brightness control, a scan-limit register that allows the user to display from one to eight digits, segment blinking that can be synchronized across drivers, and a test mode that forces all LEDs on.



II. Manufacturing Information

A. Description/Function: Serially Interfaced, +2.7V to +5.5V, 5- and 8-Digit LED Display Drivers

B. Process: TS50

C. Number of Device Transistors:

D. Fabrication Location: Taiwan

E. Assembly Location: Philippines, ThailandF. Date of Initial Production: October 27, 2001

III. Packaging Information

A. Package Type: 16-pin QSOP
B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1.3 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-3301-0005
H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per Level 1

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: 53°C/W
K. Single Layer Theta Jc: 6°C/W
L. Multi Layer Theta Ja: 44°C/W
M. Multi Layer Theta Jc: 6°C/W

IV. Die Information

A. Dimensions: 80 X 94 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None
E. Minimum Metal Width: 0.50μm
F. Minimum Metal Spacing: 0.50μm
G. Bondpad Dimensions: 5 mil. Sq.
H. Isolation Dielectric: SiO₂
I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)

Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppmD. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \underbrace{\frac{1}{\text{MTTF}}}_{\text{MTTF}} = \underbrace{\frac{1.83}{1000 \times 4340 \times 45 \times 2}}_{\text{(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)}}_{\lambda = 4.7 \times 10^{-9}}$$
$$\lambda = 4.7 \text{ F.I.T. (60% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS50 Process results in a FIT Rate of 0.25 @ 25C and 6.11 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot K210BA004L D/C 0630, Latch-Up lot K210BQ001B D/C 0115)

The DW05 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA.



Table 1Reliability Evaluation Test Results

MAX6951CEE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (No	ote 1) Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	45	0	K210BQ002Q, D/C 0347

Note 1: Life Test Data may represent plastic DIP qualification lots.