MAX685EEE
Rev. A

RELIABILITY REPORT

FOR

MAX685EEE

PLASTIC ENCAPSULATED DEVICES

November 9, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX685 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX685 DC-DC converter provides low-noise dual outputs for powering CCD imaging devices and LCDs. This device uses a single inductor to provide independently regulated positive and negative outputs. Integrated power switches are included in the small 16-pin QSOP package (same size as an 8-pin SO) to save space and reduce cost.

Each output delivers up to 10mA from a +2.7V to +5.5V input voltage range. Output voltages are set independently up to 24V and down to -9V. With a few additional low-cost components, the output voltages can be set at up to 45V and down to -16V. Output ripple magnitude is 30mVp-p. The MAX685 uses a fixed-frequency, pulse-width-modulated (PWM) control scheme at 220kHz or 400kHz to permit output noise filtering and to reduce the size of external components. The frequency can also be synchronized to an external clock signal between 200kHz and 480kHz.

The MAX685 has a power-OK indicator output (POK) that signals when both outputs are within regulation. A logic-controlled shutdown completely turns off both outputs and reduces supply current to 0.1µA. The user can also set which output turns on first.

B. Absolute Maximum Ratings

Item	Rating
V_{DD}, VP to GND	-0.3V to +6V
PGND to GND	-0.3V to +0.3V
V_{DD} to VP	-0.3V to +0.3V
LXN, POK to GND	-0.3V to +30V
LXP to V_{DD}	-15V to +0.3V
REF, SEQ, /SHDN to GND	-0.3V to (V_{DD} + 0.3V)
FBP, FBN, SYNC to GND	-0.3V to +6V
Junction Temperature	+150°C
Storage Temp.	-65°C to +165°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
16-Pin QSOP	667mW
Derates above +70°C	
16-Pin QSOP	8.3mW/°C

II. Manufacturing Information

A. Description/Function: Dual-Output (Positive & Negative) DC-DC Converter for CCD and LCD

B. Process: S12 (SG1.2) - Standard 1.2 micron silicon gate CMOS

C. Number of Device Transistors: 902

D. Fabrication Location: California or Oregon, USA

E. Assembly Location: Korea, Philippines, Thailand, Malaysia

F. Date of Initial Production: April, 1998

III. Packaging Information

A. Package Type: **16 Lead QSOP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-1101-0012

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 86 x 96 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Si

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{8.35}{192 \times 4389 \times 240 \times 2}$$ (Chi square value for MTTF upper limit)

↳ Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 20.64 \times 10^{-9}$ λ = 20.64 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5369) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PX20 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit) and +/-100V Machine Model per JEDEC Std # JESD22-A115-A. Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX685EEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	240	3
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	200	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.
Note 2: Generic Process/Package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

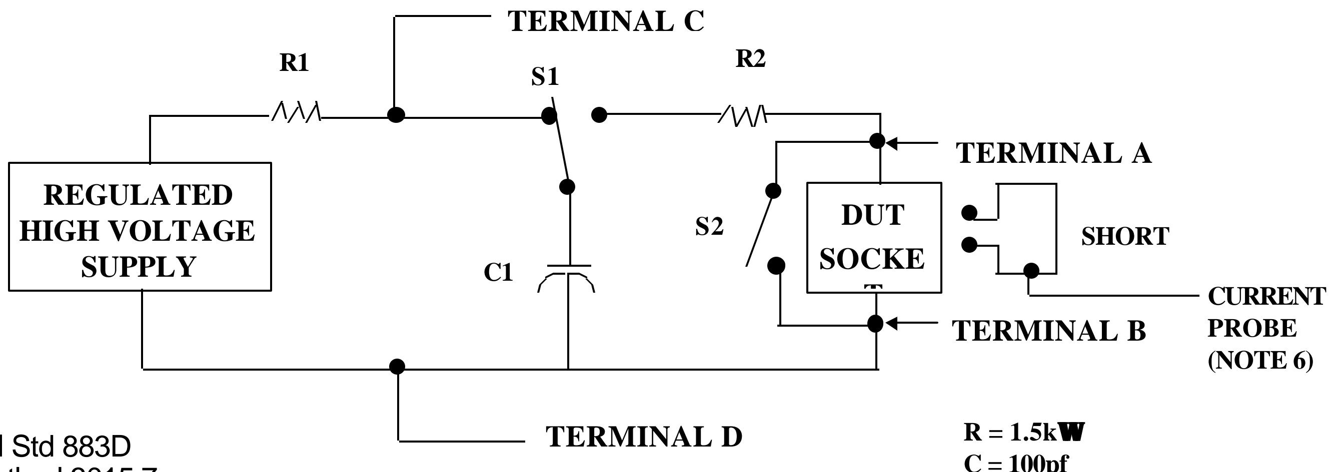
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

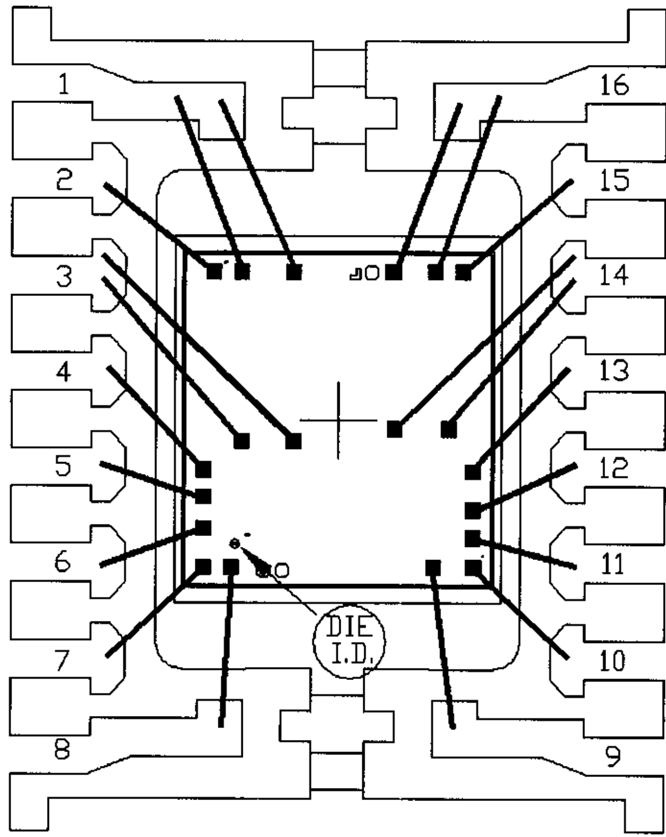
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

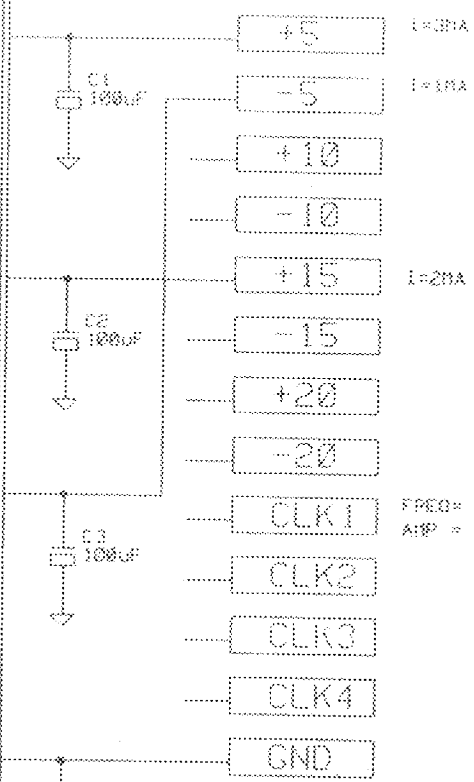
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: E16-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 96X130	PKG. DESIGN			BUILDSHEET NUMBER: 05-1101-0012	REV.: A

UNCONTROLLED DOCUMENTS



.... Steady state life test is per MIL-STD-883 Method 1005

.... Burn-in is per MIL-STD-883 Method 1015. Cond. B

NOTES:

1. Temperature: +125oC or equivalent
2. Time: 160 hours min, or equivalent
3. All components and material must stand +150oC continuous
4. Approved for [ ] Commercial
   [ ] HR/883

MAXIM	CREATED: 16-MAY-96	BY: AM	ENG1:	ENG2: -
	LAST SAVED: 12:06:51 05-31-96		SIZE B / A REVISION 00/00/00	DWG NO. 06-5369
BURNIN	PROJECT: PX20Z / DESC.: Burn-in Schematics		FILE: BURNIN.GRN	SHEET 1 OF 1