

RELIABILITY REPORT
FOR
MAX674xxx
PLASTIC ENCAPSULATED DEVICES

May 31, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

A handwritten signature in black ink, appearing to read "J Pedicord".

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

A handwritten signature in black ink, appearing to read "Bryan J. Preeshl".

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX674 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX674 is a precision voltage reference that is pretrimmed to within $\pm 0.15\%$ of 10V. This reference features excellent temperature stability (as low as 12.0ppm/ $^{\circ}\text{C}$ guaranteed), low current drain and low noise.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Input Voltage	40V
Output Short-Circuit Duration (to Ground or V_{IN})	Indefinite
Storage Temp.	-65°C to $+150^{\circ}\text{C}$
Lead Temp. (10 sec.)	$+300^{\circ}\text{C}$
Power Dissipation	300mW
Derates above $+70^{\circ}\text{C}$	5.0mW/ $^{\circ}\text{C}$
Continuous Power Dissipation ($T_A = +70^{\circ}\text{C}$)	
8-Pin PDIP	727mW
8-Pin SO	471mW
Derates above $+70^{\circ}\text{C}$	
8-Pin PDIP	9.1mW/ $^{\circ}\text{C}$
8-Pin SO	5.88mW/ $^{\circ}\text{C}$

II. Manufacturing Information

A. Description/Function:	+10V Precision Voltage Reference
B. Process:	BB5 - Standard 44V 5 micron Bipolar Process
C. Number of Device Transistors:	22
D. Fabrication Location:	Arizona, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	December, 1990

III. Packaging Information

A. Package Type:	8-Lead SO	8-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0901-0103	# 05-0901-0102
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	78 x 62 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 800 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 1.36 \times 10^{-9}$$

$$\lambda = 1.36 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-0269) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RF01-2 die type has been found to have all pins able to withstand a transient pulse of $\pm 1500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 100\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX674xxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		800	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO	77	0
			PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

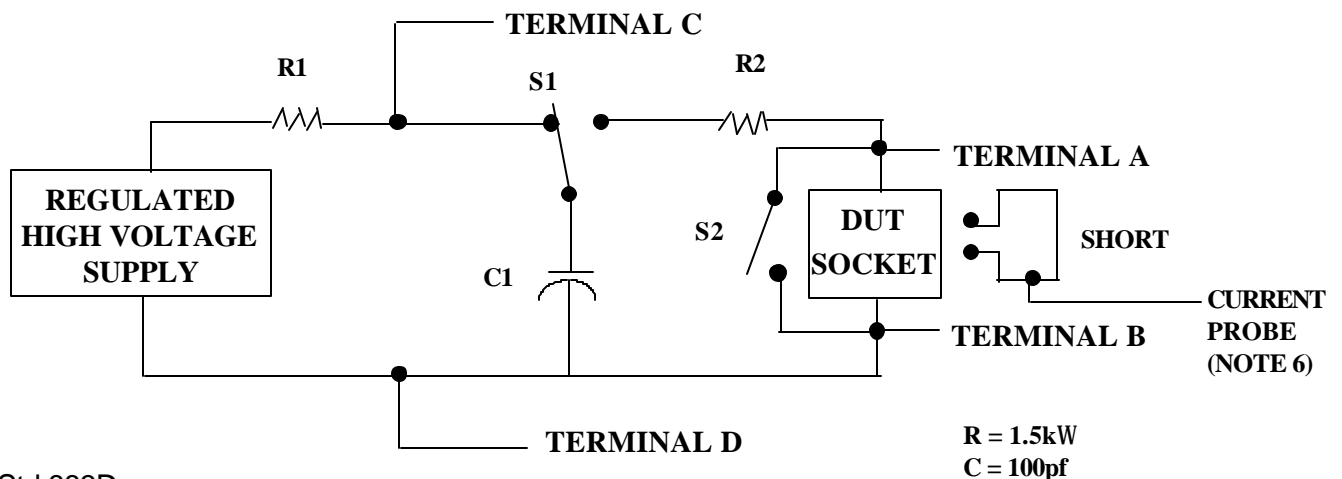
2/ No connects are not to be tested.

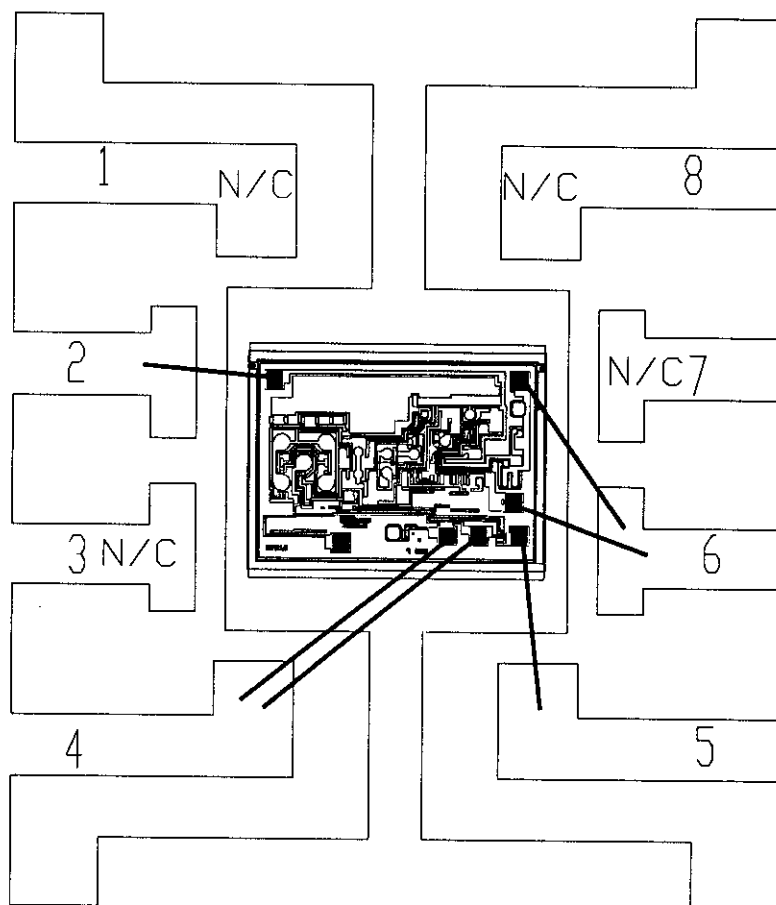
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: S8-2	
CAV./PAD SIZE: 90 X 90	PKG. DESIGN

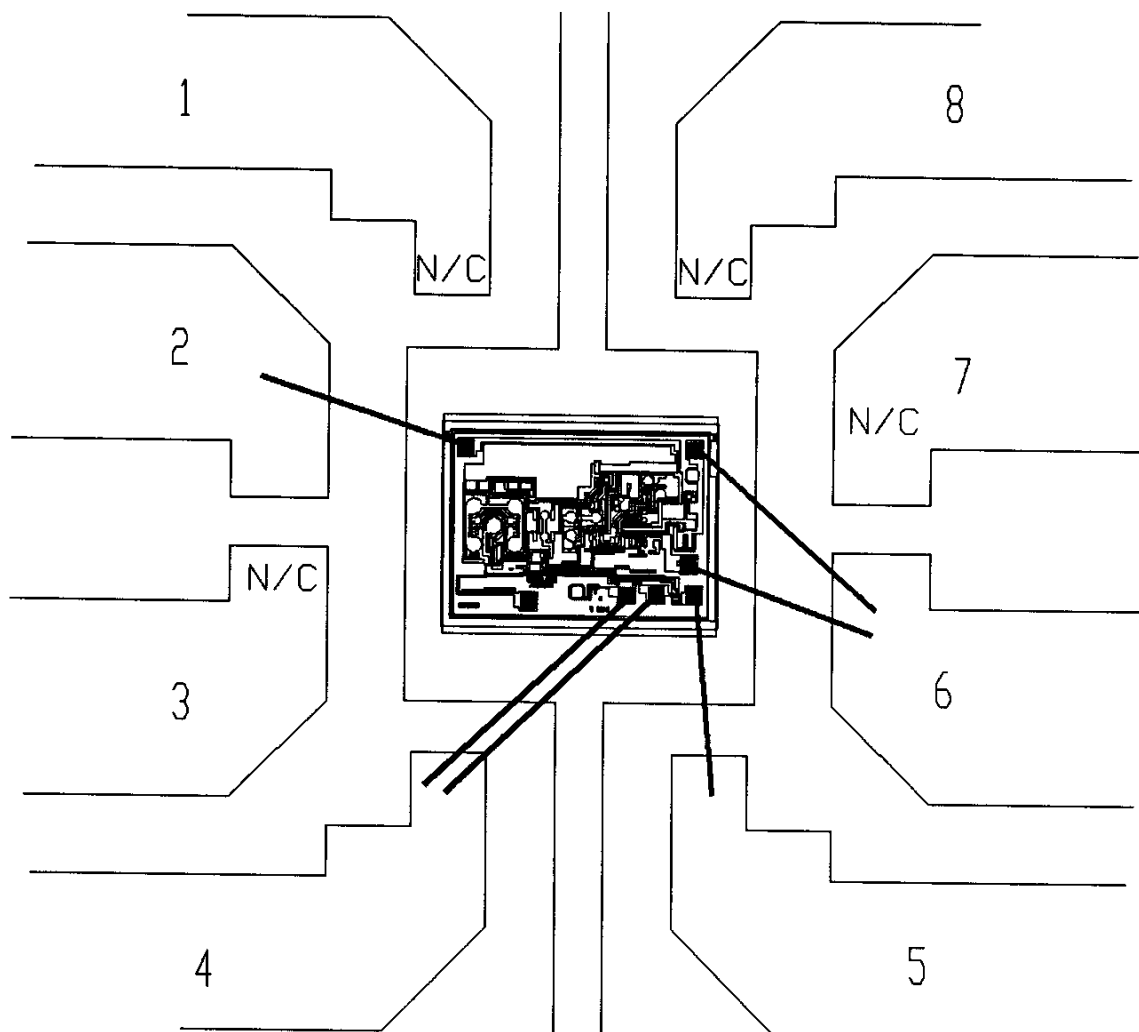
APPROVALS

DATE

MAXIM

BUILD SHEET NUMBER:
05-0901-0103

REV.:
A



PKG.CODE: P8-1

CAV./PAD SIZE:
100 X 100

APPROVALS

DATE ,

MAXIM

BUILDSHEET NUMBER:

REV.:

05-0901-0102

A

PKG.
DESIGN

