RELIABILITY REPORT

FOR

MAX6729KAxxDx

PLASTIC ENCAPSULATED DEVICES

March 5, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX6729 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6729, ultra-low-voltage microprocessor (µP) supervisory circuit is designed to monitor two system power-supply voltages. This devices asserts a system reset if any monitored supply falls below its factory-trimmed or adjustable threshold and maintain reset for a minimum timeout period after all supplies rise above their thresholds. The integrated dual supervisory circuit significantly improves system reliability and reduces size compared to separate ICs or discrete components.

This devices monitors primary supply voltages ($V_{CC}1$) from 1.8V to 5.0V and secondary supply voltages ($V_{CC}2$) from 0.9V to 3.3V with factory-trimmed reset threshold voltage options (see *Reset Voltage Threshold Suffix Guide*). This device is guaranteed to be in the correct reset output logic state when either $V_{CC}1$ or $V_{CC}2$ remains greater than 0.8V.

Select reset timeout periods from 1.1ms to 1120ms (min) (see *Reset Timeout Period Suffix Guide*). The MAX6729 are available in a small 8-pin SOT23 package and operates over the -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
Terminal Voltage (with respect to GND)	
VCC1, VCC2	-0.3V to +6V
Push-Pull RST, RST1 , PFO , RST	-0.3V to (VCC1 + 0.3V)
Push-Pull RST2	-0.3V to (VCC2 + 0.3V)
RSTIN, PFI, MR , WDI	-0.3V to +6V
Input Current/Output Current (all pins)	20mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°
Continuous Power Dissipation (TA = +70°C)	
8-Pin SOT23	714mW
Derates above +70°C	
8-Pin SOT23	8.9mW/°C

II. Manufacturing Information

A. Description/Function:	Dual Ultra-Low-Voltage SOT23 µP Supervisory Circuits
B. Process:	S8 - Standard 8 micron silicon gate CMOS
C. Number of Device Transistors:	1072
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	October, 2002

III. Packaging Information

A. Package Type:	**8-Lead SOT23**
B. Lead Frame:	Copper
C. Lead Finish:	Solcer Plate
D. Die Attach:	Non-Conductive Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0170
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	32 X 57 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/ AlCu/ TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	2.7 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 44 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 24.68 \times 10^{-9}$ $\lambda = 24.68$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-5953) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS69-1 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1

Reliability Evaluation Test Results

MAX6729KAxxDx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	44	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

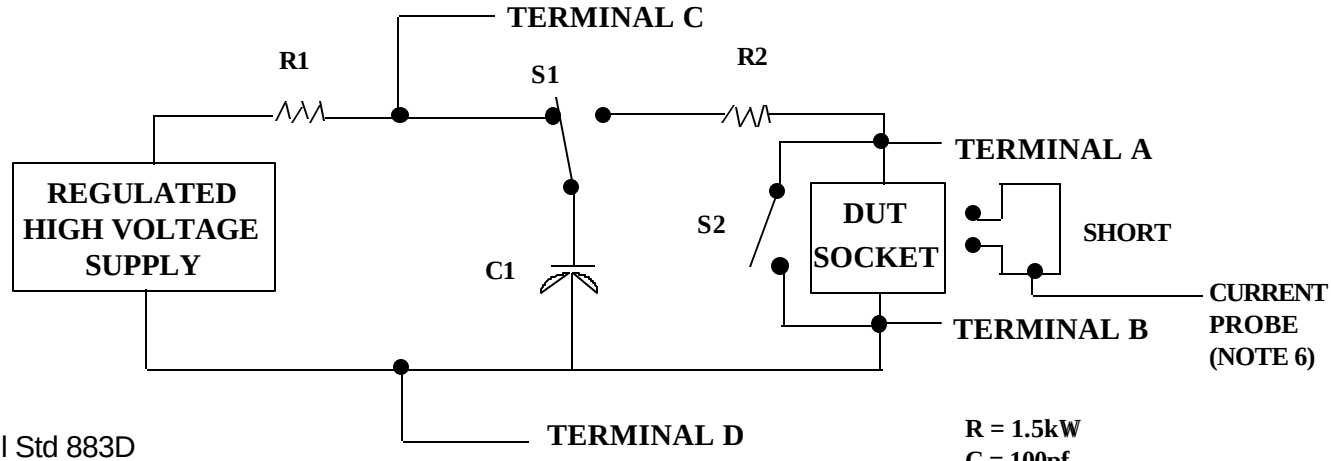
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

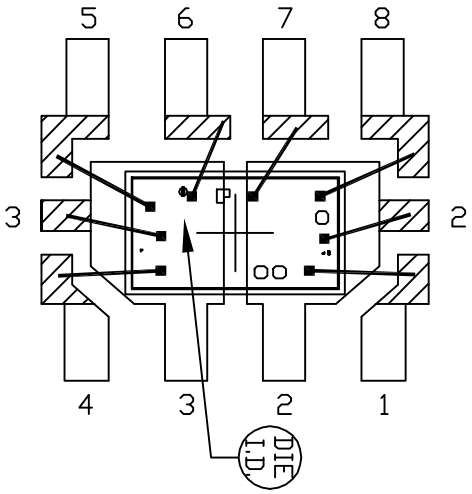
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



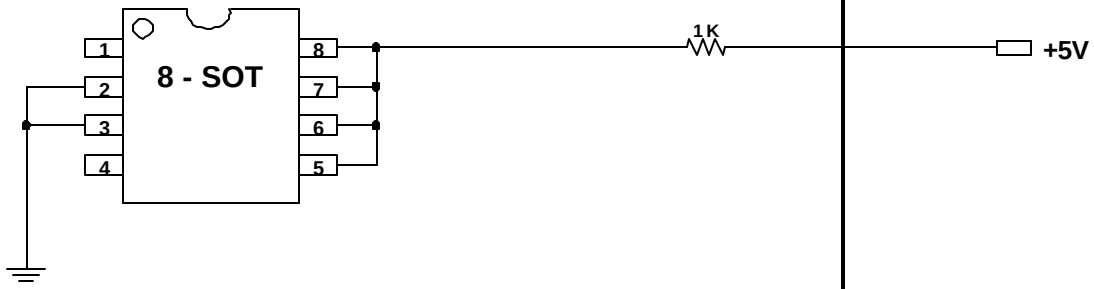
NOTE: CAVITY DOWN

BONDABLE AREA

PKG. CODE: K8S-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 75x37	PKG.			BOND DIAGRAM #: 05-1601-0170	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 6725/6726/6727/6728/6729/6734/6735

MAX. EXPECTED CURRENT = 100mA

DRAWN BY: HAK TAN

NOTES: