RELIABILITY REPORT

FOR

MAX6681MEE

PLASTIC ENCAPSULATED DEVICES

June 15, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord Quality Assurance Reliability Lab Manager Reviewed by

Bryan J. Preeshl Quality Assurance Executive Director

Conclusion

The MAX6681 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description V.Quality Assurance Information II.Manufacturing Information VI.Reliability Evaluation III.Packaging Information IV.Die InformationAttachments

I. Device Description

A. General

The MAX6681 is a precise, two-channel digital thermometer. It accurately measures the temperature of its own die and one remote PN junction and reports the temperature on a 2-wire serial interface. The remote junction can be a diode-connected transistor like the low-cost NPN type 2N3904 or PNP type 2N3906. The remote junction can also be a common-collector PNP, such as a substrate PNP of a microprocessor.

The MAX6681 includes pin-programmable default temperature thresholds for the OVERT-bar output, which provides fail-safe clock throttling or system shutdown. In addition, the device is pin programmable to select whether the OVERT-bar output responds to either the local, remote, or both temperatures.

The 2-wire serial interface accepts standard System Management Bus (SMBus)™ commands such as Write Byte, Read Byte, Send Byte, and Receive Byte to read the temperature data and program the alarm thresholds and conversion rate. The MAX6681 can function autonomously with a programmable conversion rate, which allows the control of supply current and temperature update rate to match system needs. For conversion rates of 4Hz or less, the remote sensor temperature can be represented in extended mode as 10 bits + sign with a resolution of 0.125°C. When the conversion rate is 8Hz, output data is 7 bits + sign with a resolution of 1°C. The MAX6681 also includes an SMBus timeout feature to enhance system reliability.

The MAX6681 remote accuracy is ±1°C with no calibration needed. It is available in a 16-pin QSOP package and operates throughout the -55°C to +125°C temperature range.

B. Absolute Maximum Ratings

<u>ltem</u>	Rating		
VCC	-0.3V to +6V		
DXP	-0.3V to (VCC + 0.3V)		
DXN	-0.3V to +0.8V		
SMBCLK, SMBDATA, ALERT, OVERT	-0.3V to +6V		
RESET, INT_SEL, STBY, ADD0, ADD1	-0.3V to +6V		
CRIT1, CRIT0, SENS_SEL	-0.3V to +6V		
SMBDATA, ALERT, OVERT, Current	-1mA to +50mA		
DXN Current	±1mA		
Junction Temperature	+150°C		
Storage Temperature Range	-65°C to +150°C		
Lead Temperature (soldering, 10s)	+300°C		
Continuous Power Dissipation (TA = +70°C)			
16-Pin QSOP	664mW		
Derates above +70°C			
16-Pin QSOP	8.3mW/°C		

II. Manufacturing Information

A. Description/Function: ±1°C Fail-Safe Remote/Local Temperature Sensors with SMBus Interface

B. Process: S8

C. Number of Device Transistors: 17,150

D. Fabrication Location: California, USA

E. Assembly Location: Philippines, Malaysia or Thailand

F. Date of Initial Production: March, 2002

III. Packaging Information

A. Package Type: 16-Lead QSOP

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-Filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-2901-0041

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 83 x 106 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Silicon

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Reliablity Lab Manager)
Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \underbrace{\frac{1}{\text{MTTF}}}_{} = \underbrace{\frac{1.83}{192 \times 4389 \times 45 \times 2}}_{} \text{(Chi square value for MTTF upper limit)}$$

$$\underbrace{\frac{1}{\text{Thermal acceleration factor assuming a 0.8eV activation energy}}_{}$$

$$\lambda = 24.13 \text{ x } 10^{-9}$$
 $\lambda = 24.13 \text{ F.I.T.}$ (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5891) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The TS35 die type has been found to have all pins able to withstand a transient pulse of 1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1 Reliability Evaluation Test Results

MAX6681MEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)			
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testi	ng (Note 2)			
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Str	ress (Note 2)			
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots. Note 2: Generic package/process data

Attachment #1

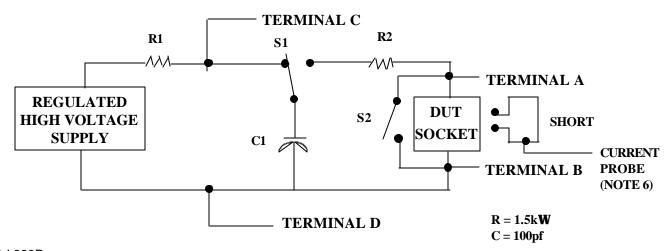
TABLE II. Pin combination to be tested. 1/2/

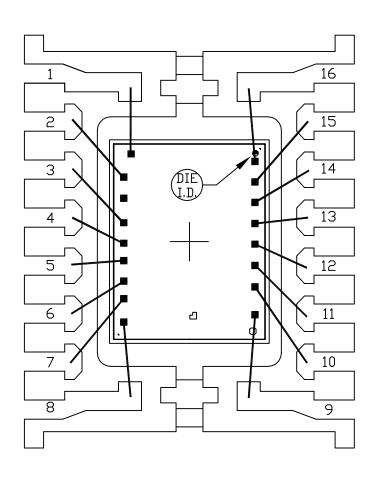
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- $\underline{3/}$ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
 - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: E16-1		SIGNATURES	DATE	CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE:	PKG.			BOND DIAGRAM #:	REV:
96X130	DESIGN			05-2901-0041	A

