MAX660xxA Rev. A

RELIABILITY REPORT

FOR

MAX660xxA

PLASTIC ENCAPSULATED DEVICES

August 23, 2003

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX660 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description II.Manufacturing Information III.Packaging Information IV.Die Information V.Quality Assurance Information VI.Reliability Evaluation

.....Attachments

I. Device Description

A. General

The MAX660 monolithic, charge-pump voltage inverter converts a +1.5V to +5.5V input to a corresponding - 1.5V to -5.5V output. Using only two low-cost capacitors, the charge pump's 100mA output replaces switching regulators, eliminating inductors and their associated cost, size, and EMI. Greater than 90% efficiency over most of its load-current range combined with a typical operating current of only 120 μ A provides ideal performance for both battery-powered and board-level voltage conversion applications. The MAX660 can also double the output voltage of an input power supply or battery, providing +9.35V at 100mA from a +5V input.

A frequency control (FC) pin selects either 10kHz typ or 80kHz typ (40kHz min) operation to optimize capacitor size and quiescent current. The oscillator frequency can also be adjusted with an external capacitor or driven with an external clock. The MAX660 is a pin-compatible, high-current upgrade of the ICL7660.

B. Absolute Maximum Ratings

ltem	Rating
Supply Voltage (V+ to GND, or GND to OUT) LV Input Voltage	+6V (OUT - 0.3V) to (V+ + 0.3V)
FC and OSC Input Voltages	The least negative of (OUT - $0.3V$) or (V+ - 6V) to (V+ + $0.3V$)
OUT and V+ Continuous Output Current	120mA
Output Short-Circuit Duration to GND (Note 1)	1sec
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin PDIP	727mW
8-Pin NSO	471mW
Derates above +70°C	
8-Pin PDIP	9.09W/°C
8-Pin NSO	5.88W/°C

Note 1: OUT may be shorted to GND for 1sec without damage, but shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above +85°C, OUT must not be shorted to GND or V+, even instantaneously, or device damage may result.

II. Manufacturing Information

A. Description/Function:	CMOS Monolithic Voltage Converter
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	88
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Korea
F. Date of Initial Production:	February, 1992

III. Packaging Information

A. Package Type:	8-Lead NSO	8-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0701-0534	# 05-0701-0533
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	73 x 120 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Jim Pedicord (Manager, Reliability Operations)
		Bryan Preeshl (Executive Director)
		Kenneth Huening (Vice President)

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{\frac{1.83}{192 \times 4389 \times 130 \times 2}}_{\text{Temperature Acceleration factor assuming an activation energy of 0.8eV}$

 $\lambda = 8.35 \times 10^{-9}$

 λ = 8.35 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-3497) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PS35 die type has been found to have all pins able to withstand a transient pulse of \pm 3000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of \pm 250mA.

Table 1 **Reliability Evaluation Test Results**

MAX660xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	(Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		130	0
Moisture Testin					
Pressure Pot	Ta = 121°C	DC Parameters	PDIP	77	0
	P = 15 psi. RH= 100% Time = 168hrs.	& functionality	NSO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stro	ess (Note 2)				
Temperature	-65°C/150°C	DC Parameters		77	0
Cycle	1000 Cycles Method 1010	& functionality			

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

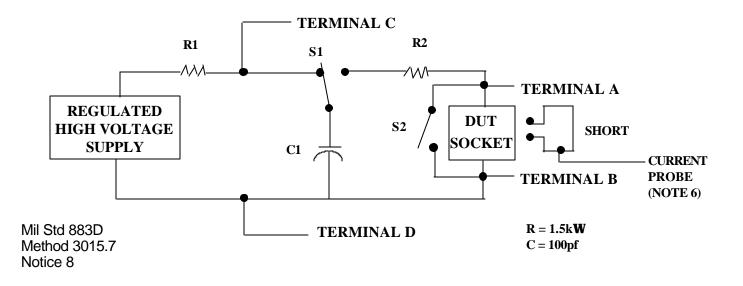
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

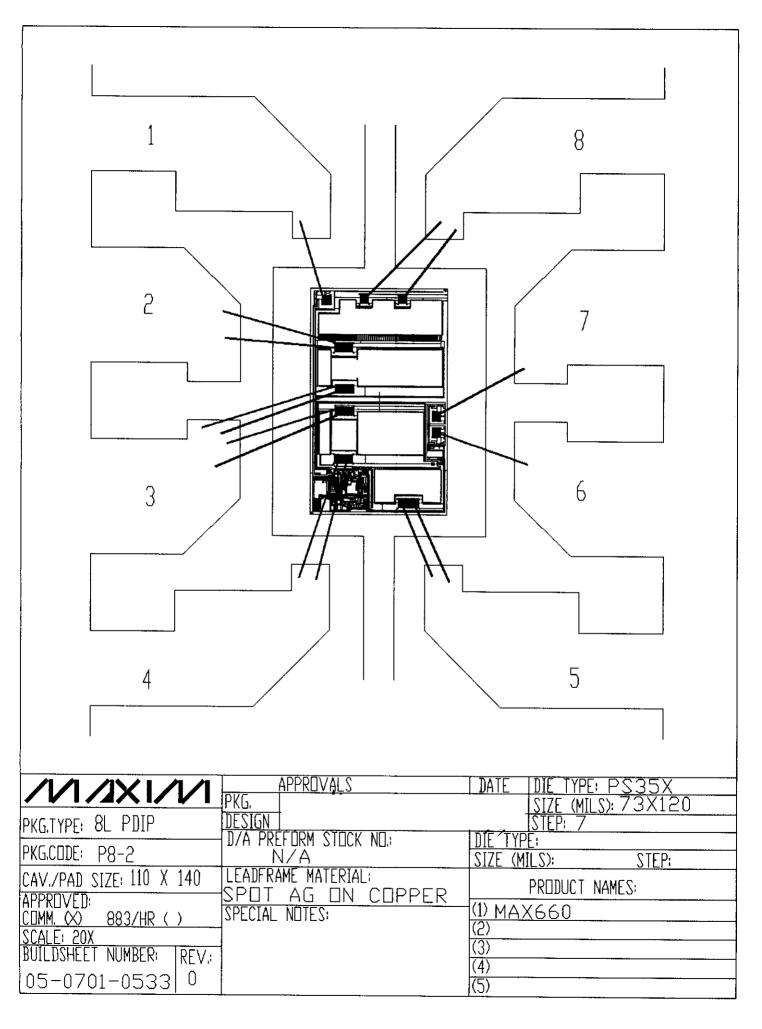
TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2/}$ No connects are not to be tested.
- $\overline{3/}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

- 3.4 Pin combinations to be tested.
 - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
 - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
 - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





////////////////////////////////////	APPROVALS PKG DESIGN D/A PREFORM STOCK NO.: N/A LEADFRAME MATERIAL: SPOT AG ON COPPER SPECIAL NOTES:	DATE DIE TYPE: P\$35X SIZE (MILS): 73X120 STEP: 7 DIE TYPE: SIZE (MILS): STEP: PRDDUCT NAMES: (1) MAX660 (2) (3) (4) (5)

