RELIABILITY REPORT

FOR

MAX6496ATA+T

PLASTIC ENCAPSULATED DEVICES

March 21, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX6496ATA+T successfully meets the quality and reliability standards required of all Maxim Integrated products, except for ESD and Latch-up. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6495-MAX6499 is a family of small, low-current, overvoltage-protection circuits for high-voltage transient systems such as those found in automotive and industrial applications. These devices monitor the input voltage and control an external n-channel MOSFET switch to isolate the load at the output during an input overvoltage condition. The MAX6495-MAX6499 operate over a wide supply voltage range from +5.5V to +72V. The gate of the n-channel MOSFET is driven high while the monitored input is below the user-adjustable overvoltage threshold. An integrated charge-pump circuit provides a 10V gate-to-source voltage to fully enhance the n-channel MOSFET. When the input voltage exceeds the user-adjusted overvoltage threshold, the gate of the MOSFET is quickly pulled low, disconnecting the load from the input. In some applications, disconnecting the output from the load is not desirable. In these cases, the protection circuit can be configured to act as a voltage limiter where the GATE output sawtooths to limit the voltage to the load (MAX6495/MAX6496/MAX6499). The MAX6496 supports lower input voltages and reduces power loss by replacing the external reverse battery diode with an external series p-channel MOSFET. The MAX6496 generates the proper bias voltage to ensure that the p-channel MOSFET is on during normal operations. The gate-to-source voltage is clamped during load-dump conditions, and the p-channel MOSFET is off during reverse-battery conditions. The MAX6497/MAX6498 feature an open-drain, undedicated comparator that notifies the system if the output falls below the programmed threshold. The MAX6497 keeps the MOSFET switch latched off until either the input power or the active-low SHDN pin is cycled. The MAX6498 will autoretry when VOVSET falls below 130mV. These devices are available in small, thermally enhanced, 6-pin and 8-pin TDFN packages and are fully specified from -40°C to +125°C.

II. Manufacturing Information

A. Description/Function:	72V, Overvoltage-Protection Switches/Limiter Controllers with an External MOSFET
B. Process:	BCD8
C. Number of Device Transistors:	566
D. Fabrication Location:	USA
E. Assembly Location:	China, Malaysia, Taiwan and Thailand
F. Date of Initial Production:	July 23, 2005

III. Packaging Information

A. Package Type:	8-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1749
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8°C/W

IV. Die Information

A. Dimensions:	61 X 75 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiW Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1 micron (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 317 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 3.5 \times 10^{-9}$

$\lambda = 3.5$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the BCD8 Process results in a FIT Rate of 0.04 @ 25C and 0.71 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The MS93 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 300V per JEDEC JESD22-A114 (lot JW1ADQ001D, D/C 0851)
ESD-CDM:	+/- 750V per JEDEC JESD22-C101 (lot JW1ADA012M, D/C 1107)

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78, except pin 3 (OVSET) and pin 5 (GATE) which pass +/- 50mA and +/- 75mA, respectively (lot JW1ADA012M, D/C 1107).

Table 1

Reliability Evaluation Test Results

MAX6496ATA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	JW1DDQ001B, D/C 0903
	Biased	& functionality	47	0	JW1ADQ001B, D/C 0851
	Time = 192 hrs.		79	0	JW1ADQ001C, D/C 0851
			47	0	NW1ABQ002B, D/C 0750
			48	0	NW1ACQ003C, D/C 0631
			48	0	NW1CBQ001B, D/C 0523

Note 1: Life Test Data may represent plastic DIP qualification lots.