

RELIABILITY REPORT  
FOR  
MAX649EPA+  
PLASTIC ENCAPSULATED DEVICES

October 10, 2014

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

|                      |
|----------------------|
| <b>Approved by</b>   |
| Sokhom Chum          |
| Quality Assurance    |
| Reliability Engineer |

## Conclusion

The MAX649EPA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX649/MAX651/MAX652 BiCMOS, step-down DC-DC switching controllers provide high efficiency over three decades of load current. A unique, current-limited pulse-frequency-modulated (PFM) control scheme gives these devices the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using only 100µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over loads ranging from 10mA to more than 2.5A. These devices use miniature external components. Their high switching frequency (up to 300kHz) allows for less than 9mm diameter surface-mount inductors. The MAX649/MAX651/MAX652 have dropout voltages less than 1V and accept input voltages up to 16.5V. Output voltages are preset at 5V (MAX649), 3.3V (MAX651), and 3V (MAX652). These controllers can also be adjusted to any voltage from 1.5V to the input voltage by using two resistors. These step-down controllers drive external P-channel MOSFETs at loads greater than 10W. If less power is required, use the MAX639/MAX640/MAX653 step-down converters with on-chip FETs, which allow up to a 225mA load current.

## II. Manufacturing Information

|                                  |   |
|----------------------------------|---|
| A. Description/Function:         | 5V/3.3V/3V or Adjustable, High-Efficiency, Low-I <sub>Q</sub> , Step-Down DC-DC Controllers |
| B. Process:                      | SG5   |
| C. Number of Device Transistors: |   |
| D. Fabrication Location:         | Oregon  |
| E. Assembly Location:            | Thailand, Philippines, Malaysia   |
| F. Date of Initial Production:   | Pre 1997  |

## III. Packaging Information

|  |                          |
|--|--------------------------|
| A. Package Type:   | 8-pin PDIP               |
| B. Lead Frame:   | Copper                   |
| C. Lead Finish:  | 100% matte Tin           |
| D. Die Attach:   | Conductive               |
| E. Bondwire:   | Au (1.3 mil dia.)        |
| F. Mold Material:  | Epoxy with silica filler |
| G. Assembly Diagram:   | #05-1701-0207            |
| H. Flammability Rating:  | Class UL94-V0            |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1                  |
| J. Single Layer Theta Ja:  | 110°C/W                  |
| K. Single Layer Theta Jc:  | 40°C/W                   |
| L. Multi Layer Theta Ja:   | N/A                      |
| M. Multi Layer Theta Jc:   | N/A                      |

## IV. Die Information

|                            |   |
|----------------------------|---|
| A. Dimensions:             | 81X106 mils   |
| B. Passivation:            | Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide) |
| C. Interconnect:           | Al/0.5%Cu with Ti/TiN Barrier   |
| D. Backside Metallization: | None  |
| E. Minimum Metal Width:    | 5.0 microns (as drawn)  |
| F. Minimum Metal Spacing:  | 5.0 microns (as drawn)  |
| G. Bondpad Dimensions:     |   |
| H. Isolation Dielectric:   | SiO <sub>2</sub>  |
| I. Die Separation Method:  | Wafer Saw   |

## V. Quality Assurance Information

- |                                   |   |
|-----------------------------------|---|
| A. Quality Assurance Contacts:    | Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA)            |
| B. Outgoing Inspection Level:     | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm  |
| D. Sampling Plan:                 | Mil-Std-105D  |

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ } 25^{\circ}\text{C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the SG5 Process results in a FIT Rate of 0.11 @ 25C and 1.96 @ 55C (0.8 eV, 60% UCL).

### B. E.S.D. and Latch-Up Testing (lot NGMDC3023A 9934)

The PW64-3 die type has been found to have all pins able to withstand a HBM transient pulse of +/-3000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX649EPA+**

| TEST ITEM                        | TEST CONDITION                          | FAILURE IDENTIFICATION           | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS             |
|----------------------------------|---|----------------------------------|-------------|--------------------|----------------------|
| <b>Static Life Test</b> (Note 1) | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 80          | 0                  | NGMFC3023B, D/C 9937 |

Note 1: Life Test Data may represent plastic DIP qualification lots