RELIABILITY REPORT

FOR

MAX6468xSxxDx

PLASTIC ENCAPSULATED DEVICES

May 26, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX6468 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

The MAX6467/MAX6468 microprocessor (µP) supervisory circuits monitor single power-supply voltages from +1.8V to +5.0V and assert a reset if the supply voltage drops below its preset threshold. An edge-triggered, one-shot manual reset function ensures that the µP enters the reset mode for a fixed timeout period only, even in the event of a continuously asserted manual reset. The MAX6467/MAX6468 significantly improve system reliability compared to traditional manual reset supervisory circuits.

A variety of factory-trimmed threshold options accommodate different supply voltages and tolerances, eliminating external components. The factory-set thresholds range from +1.575V to +4.625V to monitor +5.0V, +3.3V, +3.0V, +2.5V, and +1.8V supplies with various tolerances. Reset timeout periods of 150ms (min) and 1200ms (min) are available to accommodate different µP platforms.

A single, active-low RESET-bar output asserts when V_{CC} drops below its threshold or if the edge-triggered MR-bar asserts low. RESET-bar remains low for the reset timeout period after V_{CC} rises above its threshold and for a fixed, one-shot timeout period after a manual reset input falling edge. RESET-bar remains valid as long as V_{CC} remains above +1V. Open-drain (MAX6467) and push-pull (MAX6468) output options provide additional flexibility in the system design.

The MAX6467/MAX6468 are offered in the space-saving 4-pin SOT143 package and the ultra-small 4-pin SC70 package and are specified over the automotive (-40°C to +125°C) temperature range.

B. Absolute Maximum Ratings

Item	Rating
RESET to GND	
Open-Drain	-0.3V to +6.0V
Push-Pull	-0.3V to (VCC + 0.3V)
MR to GND	-0.3V to (VCC + 0.3V)
Input/Output Current (all pins)	20mA
Continuous Power Dissipation (TA = +70°C)	
4-Pin SC70 (derate 3.1mW/°C above +70°C)	245mW
4-Pin SOT143 (derate 4mW/°C above +70°C)	320mW
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function: Microprocessor Supervisory Reset Circuits with Edge-Triggered, One-Shot Manual Reset

B. Process:	B8 (Standard .8 micron silicon gate CMOS)
C. Number of Device Transistors:	748
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	July, 2002

III. Packaging Information

	4-Pin SOT	**4-Pin SC70**
A. Package Type:		
B. Lead Frame:	Copper or Alloy 42	Alloy 42
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy	Non-Conductive Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0186	Buildsheet # 05-1601-0187
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	30 x 31 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$

(Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.92 \times 10^{-9}$ $\lambda = 13.92$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5983) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT Rate of 0.17 @ 25C and 2.92 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS75-1 die type has been found to have all pins able to withstand a transient pulse of +/-2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX6468xSxxD

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

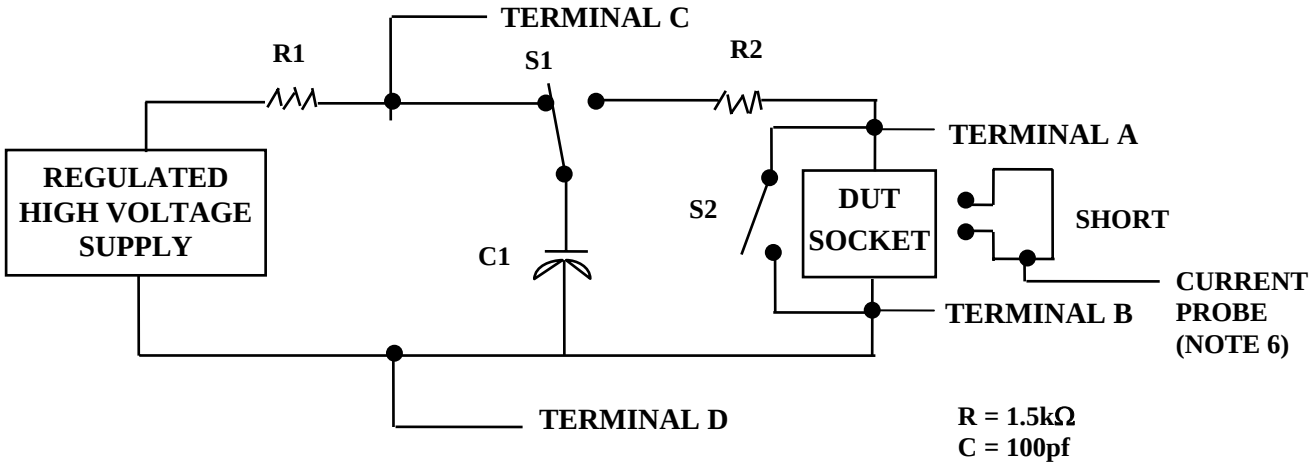
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

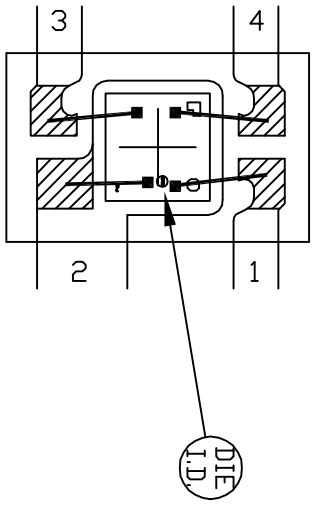
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



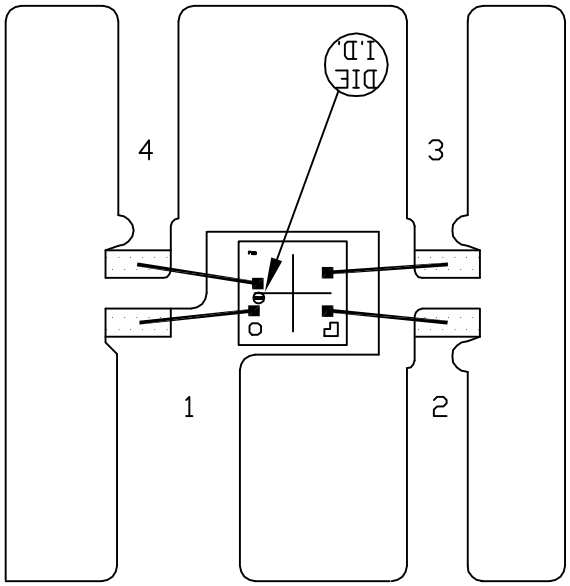


USE NON-CONDUCTIVE EPOXY

BONDABLE AREA

NOTE: CAVITY DOWN

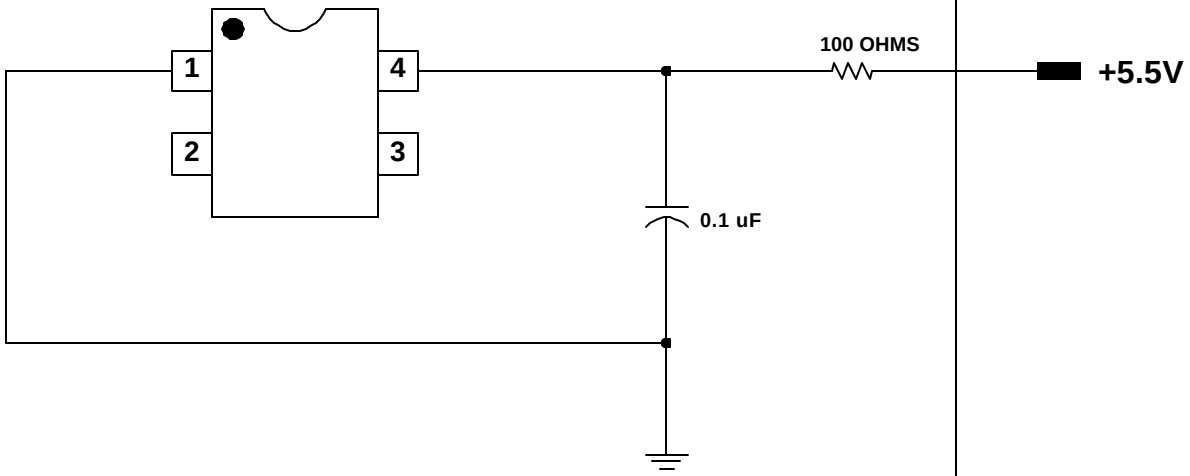
PKG. CODE: X4-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 34x35	PKG.			BOND DIAGRAM #: 05-1601-0187	REV: A
	DESIGN				



PKG. CODE: U4-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 45X32	PKG.			BOND DIAGRAM #: 05-1601-0186	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 6467/6468
PACKAGE: 4-SOT
MAX. EXPECTED CURRENT = 13uA