MAX6421xSxx
Rev. A

RELIABILITY REPORT

FOR

MAX6421xSxx

PLASTIC ENCAPSULATED DEVICES

August 4, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
Reliability Lab Manager

Conclusion

The MAX6421 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6421 low-power microprocessor supervisor circuit monitors system voltages from 1.6V to 5V. This device performs a single function: it asserts a reset signal whenever the V_{CC} supply voltage falls below its reset threshold. The reset output remains asserted for the reset timeout period after V_{CC} rises above the reset threshold. The reset timeout is externally set by a capacitor to provide more flexibility.

The MAX6421 has an active-low, push-pull reset output. The MAX6421 is offered in 4-pin SC70 or SOT143 packages.

B. Absolute Maximum Ratings

Item	Rating
All Voltages Referenced to GND	
VCC	-0.3V to +6.0V
SRT, RESET, RESET (push-pull)	-0.3V to (VCC + 0.3V)
RESET (open drain)	-0.3V to +6.0V
Input Current (all pins)	±20mA
Output Current (RESET, RESET)	±20mA
Continuous Power Dissipation (TA = +70°C)	
4-Pin SC70 (derate 3.1mW/°C above +70°C)	245mW
4-Pin SOT143 (derate 4mW/°C above +70°C)	320mW
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	Low-Power, SC70/SOT µP Reset Circuits with Capacitor-Adjustable Reset Timeout Delay
B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	295
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia, USA, or Thailand
F. Date of Initial Production:	April, 2002

III. Packaging Information

A. Package Type:	**4-Pin SC70**	**4-Pin SOT143**
B. Lead Frame:	Alloy 42	Copper or Alloy 42
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate or 100% Matte Tin
D. Die Attach:	Nonconductive Epoxy	Nonconductive Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1601-0150	# 05-1601-0151
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	31 x 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.74 \times 10^{-9}$

λ = 13.74 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5848) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The MS70 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX6421xSxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SC70 SOT	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

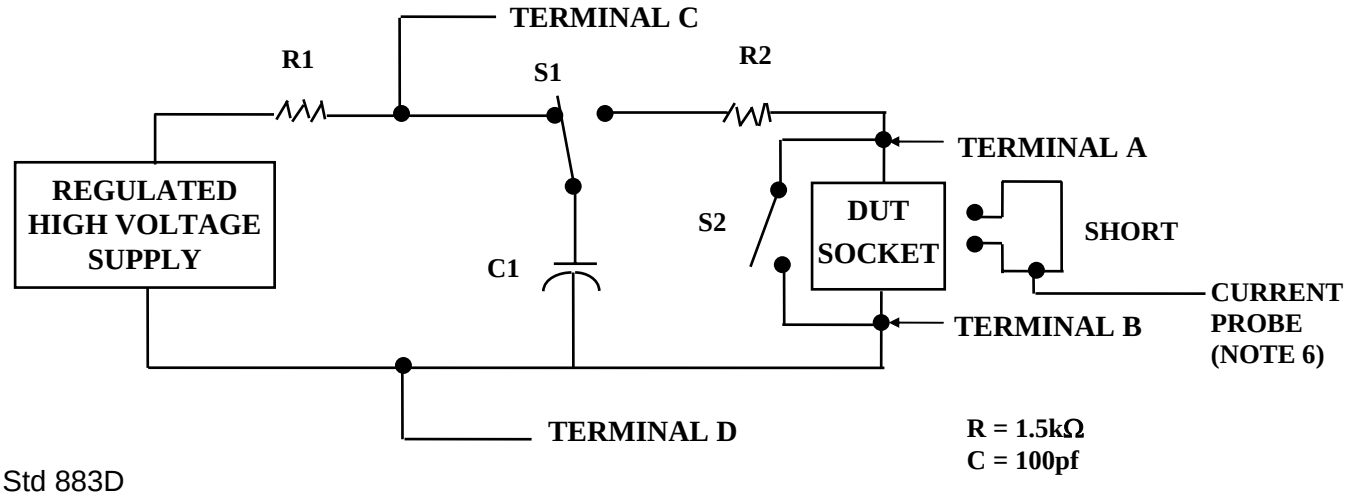
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

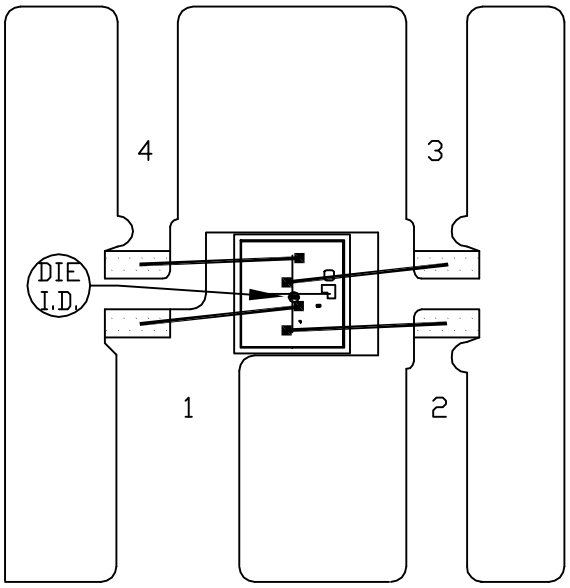
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

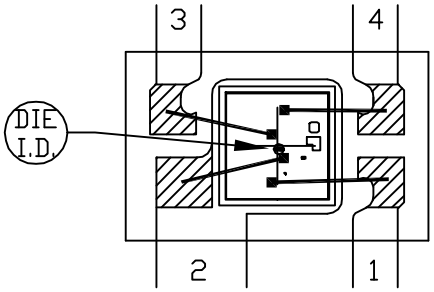
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





USE NON-CONDUCTIVE EPOXY

PKG. CODE: U4-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 45X32	PKG.			BOND DIAGRAM #: 05-1601-0151 / REV: A
	DESIGN			



USE NON-CONDUCTIVE EPOXY

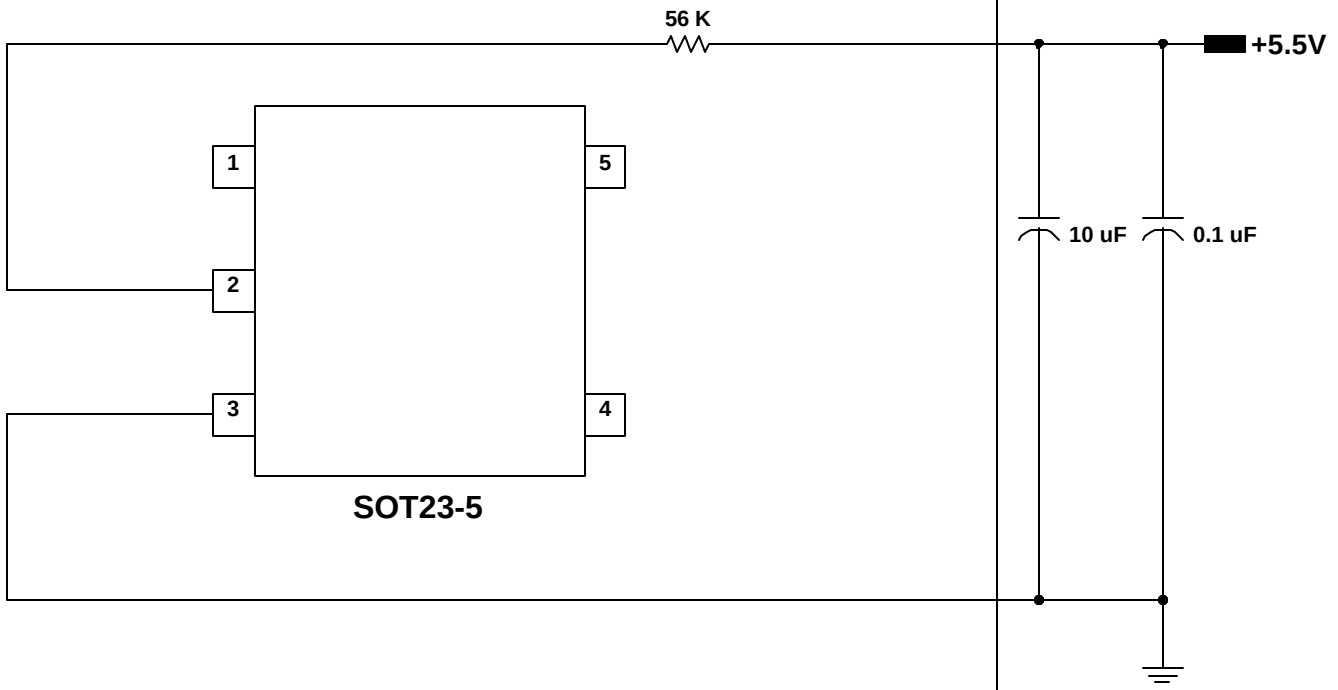
BONDABLE AREA

NOTE: CAVITY DOWN

PKG. CODE: X4-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 34x35	PKG.			BOND DIAGRAM #: 05-1601-0150	REV: B
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 6425

MAX. EXPECTED CURRENT = 100 uA