RELIABILITY REPORT

FOR

MAX6418UKxx+T

PLASTIC ENCAPSULATED DEVICES

March 5, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX6418UKxx+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6412-MAX6420 low-power microprocessor supervisor circuits monitor system voltages from 1.6V to 5V. These devices are designed to assert a reset signal whenever the VCC supply voltage or RESET IN falls below its reset threshold or the manual reset input is asserted. The reset output remains asserted for the reset timeout period after VCC and RESET IN rise above the reset threshold and the manual reset input is deasserted. The reset timeout is externally set by a capacitor to provide more flexibility. The MAX6412/MAX6413/MAX6414 feature fixed thresholds from 1.575V to 5V in approximately 100mV increments and a manual reset input. The MAX6415/MAX6416/MAX6417 are offered with an adjustable reset input that can monitor voltages down to 1.26V and the MAX6418/MAX6419/MAX6420 are offered with one fixed input and one adjustable input to monitor dual-voltage systems. The MAX6412/MAX6415/MAX6418 have an active-low, push-pull reset output. The MAX6413/MAX6416/MAX6419 have an active-high, push-pull reset output and the MAX6414/MAX6417/MAX6420 have an active-low, open-drain reset output. All of these devices are offered in a SOT23-5 package and are fully specified from -40°C to +125°C.

II. Manufacturing Information

A. Description/Function:	Low-Power, Single/Dual-Voltage µP Reset Circuits with Capacitor-Adjustable Reset Timeout Delay
B. Process:	B8
C. Number of Device Transistors:	
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia, Philippines and Thailand
F. Date of Initial Production:	January 26, 2002

III. Packaging Information

A. Package Type:	5-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1601-0178
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	324.3°C/W
K. Single Layer Theta Jc:	82°C/W
L. Multi Layer Theta Ja:	255.9°C/W
M. Multi Layer Theta Jc:	81°C/W

IV. Die Information

A. Dimensions:	36 X 36 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 90 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 12.2 \times 10^{-9}$

λ = 12.2 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.05 @ 25C and 0.90 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot J8K6EA005E, D/C 1013)

The MS60-6 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2000V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78, except pin 1 which only passes +/- 50mA.

Table 1

Reliability Evaluation Test Results

MAX6418UKxx+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45 45	0 0	J8K5E3001H, D/C 0907 J8K8E3001A, D/C 0907

Note 1: Life Test Data may represent plastic DIP qualification lots.