RELIABILITY REPORT

FOR

MAX6381XRxxDx+T / MAX6381LTxxDx+T

PLASTIC ENCAPSULATED DEVICES

January 22, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX6381XRxxDx+T / MAX6381LTxxDx+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX6381-MAX6390 microprocessor (µP) supervisory circuits monitor power-supply voltages from +1.8V to +5.0V while consuming only 3µA of supply current at +1.8V. Whenever VCC falls below the factory-set reset thresholds, the reset output asserts and remains asserted for a minimum reset timeout period after VCC rises above the reset threshold. Reset thresholds are available from +1.58V to +4.63V, in approximately 100mV increments. Seven minimum reset timeout delays ranging from 1ms to 1200ms are available. The MAX6381/MAX6384/MAX6387 have a push-pull active-low reset output. The MAX6382/MAX6385/MAX6388 have a push-pull active-high reset output, and the MAX6383/MAX6386/MAX6389/MAX6390 have an open-drain active-low reset output. The MAX6384/MAX6385/MAX6386 also feature a debounced manual reset input (with internal pullup resistor). The MAX6387/MAX6388/MAX6389 have an auxiliary input for monitoring a second voltage. The MAX6390 offers a manual reset input with a longer VCC reset timeout period (1120ms or 1200ms) and a shorter manual reset timeout (140ms or 150ms). The MAX6381/MAX6382/MAX6383 are available in 3-pin SC70 and 6-pin µDFN packages and the MAX6384-MAX6390 are available in 4-pin SC70 and 6-pin µDFN packages.

II. Manufacturing Information

A. Description/Function:	SC70/µDFN, Single/Dual Low-Voltage, Low-Power µP Reset Circuits	
B. Process:	B8	
C. Number of Device Transistors:	647	
D. Fabrication Location:	USA	
E. Assembly Location:	Malaysia and Thailand	Taiwan and Thailand
F. Date of Initial Production:	October 22, 2000	

III. Packaging Information

A. Package Type:	3-pin SC70	6-pin uDFN
B. Lead Frame:	Copper	N/A
C. Lead Finish:	100% matte Tin	Au plated
D. Die Attach:	Non-conductive	Non-conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-1601-0127	# 05-9000-2093
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	340°C/W	°C/W
K. Single Layer Theta Jc:	115°C/W	°C/W
L. Multi Layer Theta Ja:	340.4°C/W	477°C/W
M. Multi Layer Theta Jc:	120°C/W	122°C/W

IV. Die Information

A. Dimensions:	31 X 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 2.6 \times 10^{-9}$

$\lambda = 2.6$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.03 @ 25C and 0.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot J0PAF3001D, D/C 0926)

The MS58 die type has been found to have all pins able to withstand a transient pulse of

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX6381XRxxDx+T / MAX6381LTxxDx+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	80	0	D0PADQ001C, D/C 0634

Note 1: Life Test Data may represent plastic DIP qualification lots.