## RELIABILITY REPORT

FOR

## MAX6324HUTxx

PLASTIC ENCAPSULATED DEVICES

August 2, 2002

# **MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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#### Conclusion

The MAX6324H successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

#### **Table of Contents**

I. ......Device Description

II. ......Manufacturing Information

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#### I. Device Description

The MAX6324H microprocessor ( $\mu$ P) supervisory circuit monitors power supplies and  $\mu$ P activity in digital systems. A watchdog timer looks for activity outside an expected window of operation. Six laser-trimmed reset thresholds are available with ±2.5% accuracy from +2.32V to +4.63V. Valid RESET-bar output is guaranteed down to V<sub>CC</sub> = +1.2V.

The open-drain RESET-bar is asserted low when  $V_{CC}$  falls below the reset threshold, or when the manual reset input (MR-bar) is asserted low. RESET-bar remains asserted for at least 100ms after  $V_{CC}$  rises above the reset threshold or MR-bar is deasserted.

The watchdog pulse output (WDPO-bar) utilizes an open-drain configuration. It can be triggered either by a fast timeout fault (watchdog input pulses are too close to each other) or a slow timeout fault (no watchdog input pulse is observed within the timeout period). The watchdog timeout is measured from the last falling edge of watchdog input (WDI) with a minimum pulse width of 300ns. WDPO-bar is asserted for 1ms when a fault is observed. Eight laser-trimmed timeout periods are available.

The MAX6324H are offered in a 6-pin SOT23 package and operate over the extended temperature range (-40°C to +85°C).

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#### B. Absolute Maximum Ratings

| <u>Item</u>                               | <u>Rating</u>   |  |
|---|-----------------|--|
| Terminal Voltage (with respect to GND)    |                 |  |
| VCC                                       | -0.3V to +6.0V  |  |
| WDPO , RESET (MAX6324)                    | -0.3V to +6.0V  |  |
| Input Current, VCC, WDI, MR               | 20mA            |  |
| Output Current, RESET, WDPO               | 20mA            |  |
| Rate of Rise, VCC                         | 100V/μs         |  |
| Operating Temperature Range               | -40°C to +125°C |  |
| Junction Temperature                      | +150°C          |  |
| Storage Temperature Range                 | -65°C to +150°C |  |
| Lead Temperature (soldering, 10s)         | +300°C          |  |
| Continuous Power Dissipation (TA = +70°C) |                 |  |
| 6-Pin SOT23                               | 696W            |  |
| Derates above +70°C                       |                 |  |
| 6-PIN SOT23                               | 8.7mW/°C        |  |
|   |                 |  |

## **II. Manufacturing Information**

A. Description/Function: µP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

B. Process: S8

C. Number of Device Transistors: 1371

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia or Thailand

F. Date of Initial Production: October, 2000

## III. Packaging Information

A. Package Type: 6-Lead SOT

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-Filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-1601-0091

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

## IV. Die Information

A. Dimensions: 57 x 35 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Silicon

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO<sub>2</sub>

I. Die Separation Method: Wafer Saw

#### V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Reliablity Lab Manager) Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

#### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \text{ x } 4389 \text{ x } 240 \text{ x } 2}$$
 (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

 $\lambda = 4.52 \text{ x } 10^{-9}$   $\lambda = 4.52 \text{ F.I.T.}$  (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5527) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

#### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

## C. E.S.D. and Latch-Up Testing

The MS38-7 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2500$ V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250$ mA and/or  $\pm 20$ V.

# Table 1 Reliability Evaluation Test Results

# MAX6324HUTxx

| TEST ITEM            | TEST CONDITION  | FAILURE<br>IDENTIFICATION        | SAMPLE<br>SIZE | NUMBER OF<br>FAILURES |
|----------------------|---|----------------------------------|----------------|-----------------------|
| Static Life Test     | •   |                                  |                |                       |
|                      | Ta = 135°C<br>Biased<br>Time = 192 hrs.                 | DC Parameters & functionality    | 240            | 0                     |
| Moisture Testin      | ng (Note 2)   |                                  |                |                       |
| Pressure Pot         | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | 77             | 0                     |
| 85/85                | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs.      | DC Parameters<br>& functionality | 77             | 0                     |
| Mechanical Str       | ess (Note 2)  |                                  |                |                       |
| Temperature<br>Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010               | DC Parameters                    | 77             | 0                     |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots. Note 2: Generic package/process data

#### Attachment #1

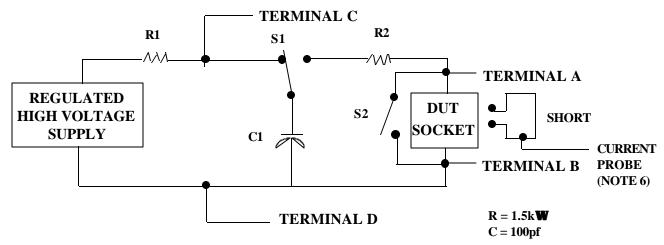
TABLE II. Pin combination to be tested. 1/2/

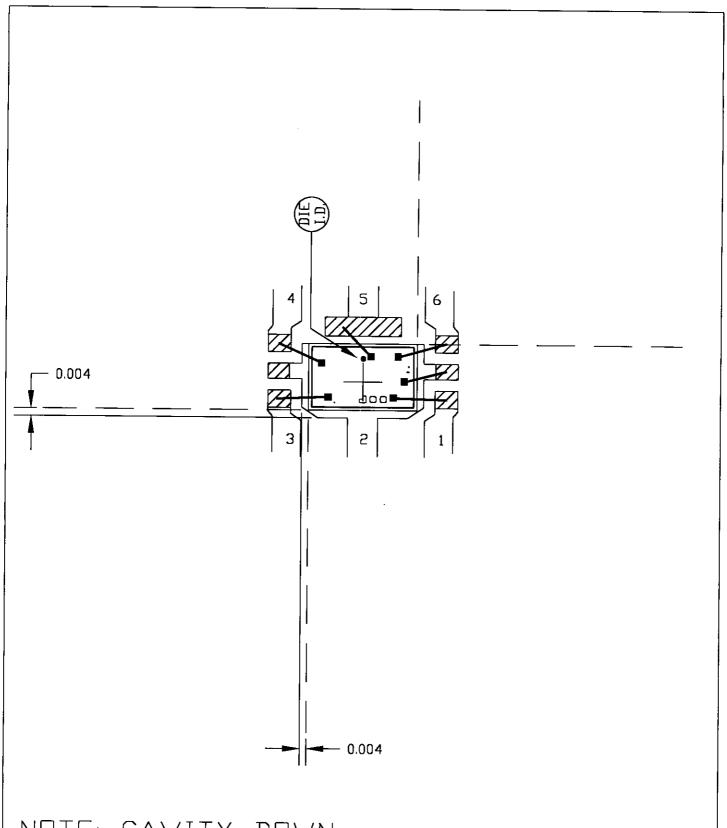
|    | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|----|--|--|
| 1. | All pins except V <sub>PS1</sub> 3/  | All V <sub>PS1</sub> pins  |
| 2. | All input and output pins  | All other input-output pins  |

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- Repeat pin combination I for each named Power supply and for ground (e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_{S}$ ,  $-V_{S}$ ,  $V_{REF}$ , etc).

#### 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
  - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





NOTE: CAVITY DOWN

| PKG.CODE: | U6-1  |        |  |
|-----------|-------|--------|--|
| CAV./PAD  | SIZE: | PKG.   |  |
|           | 64×39 | DESIGN |  |

APPROVALS DATE



05-1601-0091

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