MAX630xxA Rev. A

**RELIABILITY REPORT** 

FOR

## MAX630xxA

PLASTIC ENCAPSULATED DEVICES

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# **MAXIM INTEGRATED PRODUCTS**

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#### Conclusion

The MAX630 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

A. General

Maxim's AX630 CMOS DC-DC regulator is designed for simple, efficient, minimum size DC-DC converter circuits in the 5 milliwatt to 5 watt range. The MAX630 provides all control and power handling functions in a compact &pin package: a 1.31V bandgap reference, an oscillator, a voltage comparator, and a 375mA N channel output MOSFET. A comparator is also provided for low battery detection.

Operating current is only 70uA and is nearly independent of output switch current or duty cycle. A logic level input shuts down the regulator to less than 1uA quiescent current. Low current operation ensures high efficiency even in low power battery operated systems. The MAX630 is compatible with most battery voltages, operating from 2.0V to 16.5V.

The device is pin compatible with the Raytheon bipolar circuits RC4191/2/3, while providing significantly improved efficiency and low voltage operation

#### B. Absolute Maximum Ratings

ltem	Rating
Supply Voltage Input Voltage (Pins 1,2,6,7) Output Voltage Lx and LBD Lx Output Current	+18V -0.3V to VS+0.3V 18V 525mA Peak
LBD Output Current Continuous Power Dissipation (TA = +70°C)	50mA
8-Pin SO 8-Pin DIP	471mW 727mW
Derates above +70°C 8-Pin SO 8-Pin DIP	5.9 mW/°C 9.10mW/°C

## II. Manufacturing Information

A. Description/Function:	CMOS Micropower Step-Up Switching Regulator
B. Process:	M6 (SMG) - 6 micron metal gate CMOS
C. Number of Device Transistors:	245
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	October, 1986

# III. Packaging Information

A. Package Type:	8-Lead Small Outline	8-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0701-0570	# 05-0701-0568
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

## **IV. Die Information**

A. Dimensions:	70 x 93 mils
B. Passivation:	$Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	6 microns (as drawn)
F. Minimum Metal Spacing:	6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

### V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Jim Pedicord (Manager, Rel Operations)
		Bryan Preeshl (Executive Director)
		Kenneth Huening (Vice President)

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

#### **VI. Reliability Evaluation**

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{\frac{6.21}{192 \times 4389 \times 1599}}_{\text{Temperature Acceleration factor assuming an activation energy of 0.8eV}$ 

 $\lambda = 2.30 \times 10^{-9}$ 

 $\lambda$  = 2.30 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's eliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-1802) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

## B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

## C. E.S.D. and Latch-Up Testing

The PS04 die type has been found to have all pins able to withstand a transient pulse of  $\pm 3000$ V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 100$ mA.

## Table 1 Reliability Evaluation Test Results

## MAX630xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		1599	2
Moisture Testin	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO DIP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

# Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V <sub>PS1</sub> <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2/}$  No connects are not to be tested.
- $\overline{3/}$  Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND, + $V_{S}$ , - $V_{S}$ ,  $V_{REF}$ , etc).

- 3.4 <u>Pin combinations to be tested.</u>
  - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
  - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V<sub>SS1</sub>, or V<sub>SS2</sub> or V<sub>SS3</sub> or V<sub>CC1</sub>, or V<sub>CC2</sub>) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
  - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







