MAX604xxA Rev. A

RELIABILITY REPORT

FOR

MAX604xxA

PLASTIC ENCAPSULATED DEVICES

July 14, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

/en

Jim Pedicord Quality Assurance Manager, Reliability Operations

Conclusion

The MAX604 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX604 low-dropout, low quiescent current, linear regulator supplies 5V, 3.3V, or an adjustable output for currents up to 500mA. It is available in a 1.8W SO package. Typical dropouts are 320mV at 5V and 500mA, or 240mV at 3.3V and 200mA. Quiescent currents are 15µA typ and 35µA max. Shutdown turns off all circuitry and puts the regulator in a 2µA off mode. A unique protection scheme limits reverse currents when the input voltage falls below the output. Other features include foldback current limiting and thermal overload protection.

The output is preset at 3.3V for the MAX604. In addition, the device employs Dual Mode[™] operation, allowing useradjustable outputs from 1.25V to 11V using external resistors. The input voltage supply range is 2.7V to 11.5V.

The MAX604 features a 500mA P-channel MOSFET pass transistor. This transistor allows the devices to draw less than 35µA over temperature, independent of the output current. The supply current remains low because the P-channel MOSFET pass transistor draws no base currents (unlike the PNP transistors of conventional bipolar linear regulators). Also, when the input-to-output voltage differential becomes small, the internal P-channel MOSFET does not suffer from excessive base current losses that occur with saturated PNP transistors.

B. Absolute Maximum Ratings

Item

Supply Voltage (IN or OUT to GND) Output Short-Circuit Duration Continuous Output Current SET, OFF Input Voltages (IN + 0.3V) or (OUT + 0.3V) Continuous Power Dissipation (TA = +70°C) Plastic DIP (derate 9.09mW/°C above +70°C) SO (derate 23.6mW/°C above +70°C) Operating Temperature Ranges MAX60_C_A MAX60_E_A Junction Temperature Storage Temperature Range Lead Temperature (soldering, 10sec) Rating

-0.3V to +12V 1 min 600mA -0.3V to the greater of

727mW 1.8W

0°C to +70°C -40°C to +85°C +150°C -65°C to +160°C +300°C

II. Manufacturing Information

A. Description/Function:	5V/3.3V or Adjustable, Low-Dropout, Low IQ, 500mA Linear Regulators
B. Process:	S3 - Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	111
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	May, 1995

III. Packaging Information

A. Package Type:	8-pin Plastic Dip	8-pin SO
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate or 100% Matte Tin
D. Die Attach:	Non-Conductive Epoxy	Non-Conductive Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1701-0189	# 05-1701-0193
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
 Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: 	Level 1	Level 1

IV. Die Information

A. Dimensions:	96 x 104 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord Bryan Preeshl (Manager, Reliability Operations) (Managing Director of QA)

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \text{ x } 4340 \text{ x } 290 \text{ x } 2}$ (Chi square value for MTTF upper limit) Temperature Acceleration factor assuming an activation energy of 0.8eV

 $\lambda = 3.79 \text{ x } 10^{-9}$ $\lambda = 3.79 \text{ F.I.T.}$ (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5123) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S3 Process results in a FIT Rate of 0.15 @ 25C and 2.60 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PW50-1 die type has been found to have all pins able to withstand a transient pulse of $\pm 2000V$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1 Reliability Evaluation Test Results

MAX604xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		290	0
Moisture Testi	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO PDIP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical St	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\frac{32}{2}$ No connects are not to be tested. $\frac{32}{2}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{RFF} , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected a. to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination b. of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of C. all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





USE NON-CONDUCTIVE EPOXY 84-3J ONLY

PKG.CODE: S8-7F	
CAV./PAD SIZE:	PKG.
114X110	DESIGN

DATE

APPROVALS



